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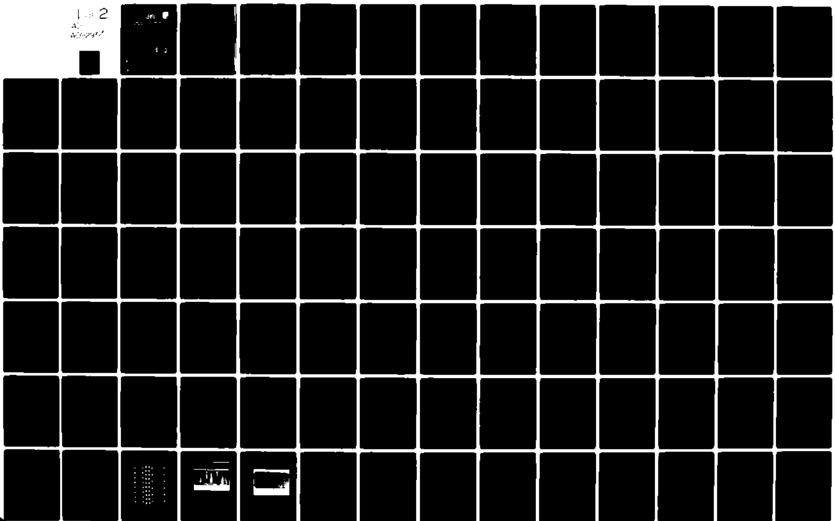

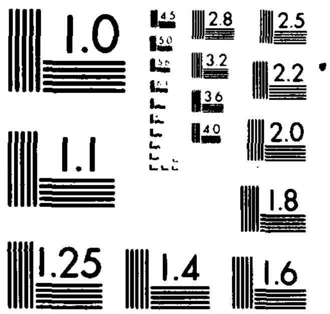

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HYBRID MICROCIRCUIT REWORK PROCEDURES EVALUATION

Hughes Aircraft Company

G. T. Malloy

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The objective of this program is to make a comprehensive assessment of all factors related to the rework of hybrid microcircuits and how these factors affect hybrid reliability. Based on this assessment, rework, criteria and guidelines have been prepared for inclusion in MIL-M-38510.

The program effort consisted of two major tasks:

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Item 20 (Cont'd)

(1) A review of the hybrid microcircuit literature and a survey of 21 manufacturers of military grade hybrids, to determine the common practices and in-process controls used and problems encountered in hybrid manufacturing.

(2) An experimental evaluation of the reliability of reworked vs non-reworked test specimen hybrids.

The test phase of the program utilized the effects of mechanical and thermal stresses, applied as conventional MIL-STD-883 environmental test exposure, to measure the effects of one, two or more rework cycles on wire bond degradation or failure.

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CONTENTS (Continued)

EVALUATION

The objective of this effort which supports RADC TPO 4F.1 Solid State Device Reliability was to evaluate existing military hybrid microcircuit vendors rework procedures, and revise where necessary the workmanship criteria of MIL-M-38510, "General Specification for Microcircuits". Special emphasis was placed on determining the cumulative effect of performing various types of rework during the fabrication of hybrid microcircuits.

Study results describe the various materials, manufacturing processes and techniques used in fabricating hybrids and the procedures used for the rework of hybrids in detail. Conclusions drawn from the testing phase of this effort and a survey of hybrid field failure data indicate that properly selected, documented and controlled rework will not have a significant adverse effect on device reliability. Comparisons have been made of many rework factors indicating both good and bad features. For example, seam welding of the lid to the package is the preferred technique when package delidding and resealing is performed, while metallic die mounting rework and the use of flux can present a reliability risk.

Based on this effort RADC is presently preparing and will coordinate new hybrid microcircuit rework procedures for inclusion in MIL-M-38510 which will significantly change the existing criteria. Rework will be redefined, ground rules for the use of the new criteria will be generated and the requirement to document and certify all rework procedures will be recommended. These new procedures should increase the yield, thereby decreasing the cost without degrading the reliability of hybrid microcircuits used in military systems.

John P Farrell

JOHN P. FARRELL
Project Engineer

1.0 INTRODUCTION

1.1 General. In the last decade, both military and commercial electronic systems have experienced a steady increase in the quantity of hybrids used. In spite of the increased application of military grade hybrid microcircuits, the number of units produced per type and per production run remains relatively small. Therefore, mass production techniques have, in general, not been found to be economically justifiable, and as a consequence, hybrid unit costs remain high. Hybrids that fail at various stages of the manufacturing and testing processes are too expensive to discard; in addition, replacement delays, which generally run into a few months or more, can endanger the timely delivery of a system. For these two main reasons (i.e., cost impact and schedule impact), the majority of military type hybrid microcircuit manufacturers has found that repair and/or rework of hybrids is a requisite for parts that have failed during the production or testing phases. These phases precede, or are a part of, production acceptance testing prior to shipment.

1.2 Objective. Although it is evident that rework can significantly reduce costs and schedule time, these procedures must not compromise the reliability of the end product. Package delidding for rework purposes is proscribed by MIL-M-38510, the general specification for military and space grade microcircuits.

The objective of this program was the modification of existing MIL-M-38510 rework requirements and the establishment of rework guidelines that are compatible with state-of-the-art hybrid microcircuits.

The program objective was attained by conducting a comprehensive assessment of all the known factors related to the rework of hybrid microcircuits that could affect their long-term reliability. Based on this assessment, hybrid microcircuit rework criteria and guidelines were prepared for incorporation into MIL-M-38510.

1.2.1 Definition of rework. One of the goals of this program was to develop a comprehensive definition of the concept of hybrid rework.

According to MIL-STD-1520A, Reworked Material is defined as "Material that was non-conforming but has been subjected to a process that restores all non-conforming characteristics to the requirements in the contract, specification, drawing, or other approved product description."

It was deemed advisable to define hybrid microcircuit rework at the outset of the program. A typical face-up chip and wire hybrid manufacturing process sequence was used as the vehicle to develop the definition:

> Hybrid Microcircuit Rework is the repeating of a previous manufacturing process step and is performed to replace (or improve the condition of) a defective or out-of-specification hybrid microcircuit element. It consists of the correction or removal (and replacement) of defective hybrid components as determined by in-process screening tests, visual inspection and electrical tests. These corrective procedures may be employed either before or after package sealing to eliminate the condition of nonconformance with the specification, drawing or other approved product description.

Repair, on the other hand, is defined as the application of a corrective procedure that reduces but does not eliminate the condition of non-conformance with the specification, drawing or other approved requirement.

1.3 Approach. The technical procedure of this program was to assess the effects of mechanical and thermal stresses (applied as conventional MIL-STD-883 environmental screening) on the various elements of hybrid microcircuits, to permit a comparison of the reliability of the as-assembled versus the replaced/reworked hybrids.

The Reliability criteria utilized in this program consisted of determination of the effects of mechanical and thermal stresses on changes in wire bond strength and wire bond electrical resistance.

Specifically, the experimental technique was based on the detection of wire bond degradation and failures during environmental testing. The methods used permitted determination of (a) the quantity of lifted wire bonds,

(b) change in the wire bond electrical resistance by measuring the increase in resistance along a row of shorted, series resistors, and (c) the change in wire bond pull strength. The test vehicle selected to determine the effects of rework on hybrid reliability was a simulated hybrid microcircuit test specimen, containing three thick film or three thin film substrates with attached active and passive devices.

The program was divided into five individual tasks, consisting of:

Task I. Package Delidding and Resealing

(a) Solder seals - hand soldered and preform seam "brazed" (hard solder).

(b) Welded seals.

Task II. Eutectic Attachment Rework

(a) Die replacement

(b) Substrate replacement

Task III. Polymer Attachment Rework

(a) Die replacement

(b) Substrate replacement

Task IV. Interconnection Rework

(a) Gold and aluminum wires

(b) Beam leads

(c) Flip chip interconnects

Task V. Package Replacement

Each of the five tasks consisted of:

(a) A literature review and survey of common practices, controls and problems encountered by hybrid manufacturers. The manufacturer survey was restricted to producers of military grade hybrids. The extensive literature survey was aided by computer search.

(b) Design of the experiment and definition of the parameters to be tested. Beam leads and flip chip interconnects were not evaluated experimentally.

(c) Parts acquisition, hybrid test specimen fabrication and execution of the experiment.

(d) Analysis of the test data.

The test program was integrated to include the variables of Tasks I through V. After fabrication of the test specimens, they were divided into three groups. The three groups of test specimen hybrids were then subjected to different sequences of tests, as explained in Section 5.0. Each of the three test sequences contained a group of control specimens which were not subjected to rework. In addition, each of the three test sequences was further subdivided into smaller subgroups to permit the evaluation of the effects of one, two or more rework cycles.

After analysis of the test results and review of the literature and manufacturer survey data, each proposed rework process was subjected to the following evaluation:

(a) Effect of the rework process on hybrid reliability and the degree of risk associated with the rework process.

(b) Determination of rework controls to be imposed in the fabrication and/or test procedures: nature, extent and location of the proposed controls.

(c) Tests required to verify the adequacy and reliability of each rework process.

2.0 SUMMARY

The program effort consisted of two phases:

(1) A review of the hybrid microcircuit literature and a survey of 21 manufacturers of military grade hybrids, to determine the common practices and in-process controls used and problems encountered in hybrid production.

(2) An experimental evaluation of the reliability of reworked versus non-reworked test specimen hybrids.

The test phase of the program utilized the effects of mechanical and thermal stresses, applied as conventional MIL-STD-883 environmental test exposure, to determine the effects of one, two or more rework cycles on wire bond degradation or failure.

The most significant findings of this program are:

(1) Seam welded packages, with covers carefully removed by a milling technique, may be resealed up to three times. Glass bead cracking, initiated during the rework process, may cause degradation in leak rate.

(2) The best die-to-substrate metallization bonds are obtained using eutectic alloys (Au/Si, Au/Sn), whereas the soft solders of the Pb/Sn and Pb/Sn/Ag systems produce unsatisfactory die bonds. Rework of soft solder bonded molytab-mounted silicon chips is limited metallurgically, due to solder oxidation and solder scavenging/leaching.

(3) Experience and test results obtained from the rework evaluation of this program, from the field and from the literature, indicate that if epoxy materials are carefully selected prior to use, reliable device-to-substrate bonds may be obtained in low power hybrid microcircuits.

(4) The thermosonic gold wire bonding process allows a wider variation in bonding parameters than does thermocompression bonding.

(5) The reliability of hybrids is not affected by the replacement of packages in which the substrates are attached by epoxy.

3.0 REVIEW OF THE LITERATURE ON HYBRID MICROCIRCUIT FABRICATION AND REWORK TECHNIQUES

3.1 General. The objective of this task was to assess the various rework procedures used in hybrid manufacture and to examine the problems associated with these rework techniques. In particular, the literature review consisted of a summary and analysis of the various types of hybrid fabrication equipment, assembly materials, metallization systems, device types and handling procedures believed to be best suited for manufacture and repair of military grade hybrid microcircuits. This analysis also served as a guide to the limits of hybrid rework and, in many instances, indicated the effects of the rework process on hybrid reliability.

The literature survey was carried out using a computer aided search of the following information sources:

(a) Hughes Aircraft Company reports

(b) Defense Documentation Center reports

(c) NASA reports

(d) Open literature: IEEE Reliability Physics Proceedings, ISHM Symposia proceeding, IEEE Transactions and various other journals that cover hybrid microcircuit technology.

The open literature search was also performed in part using the Lockheed DIALOG on-line information retrieval system. Since the objective of Task IV (Interconnection Rework) includes identification of the various types of interconnection processes which are most commonly used in hybrids, and are subject to the controls of MIL-M-38510 and MIL-STD-883, the literature search was not restricted to face-up chip and wire hybrids. A review of the recent literature on flip chip and beam lead interconnection techniques was also made.

3.2 Task I - Package delidding and resealing.

3.2.1 General. Techniques for hermetically sealing hybrid microcircuits have been categorized into three groups. The three classifications, and their respective sub-classes, are listed as follows:

(a) Soldering and Brazing Methods

(1) Manual (soldering iron)

(2) Furnace (infrared)

(3) Peripheral

(4) Parallel seam

(b) Welding Methods

(1) Parallel seam

(2) Resistance

(3) Cold weld

(4) Electron Beam

(5) Laser

(6) Ultrasonic.

(c) Glass Sealing Methods

(1) Crystallizing (devitrifying) type, using a glass-ceramic or solder glass

(2) Vitreous type.

The soldering and brazing classification can be reclassified also on the basis of the alloys commonly used:

(a) Copper/silver brazing alloy (M.P. = 779°C)

(b) 80 percent gold/20 percent tin solder (M.P. = 280°C)

(c) 96 percent tin/4 percent silver solder (M.P. = 221°C)

(d) 10 percent tin/88 percent lead/2 percent silver solder (M.P. = 299°C)

(e) 62 percent tin/36 percent lead/2 percent silver solder (M.P. = 189°C)

Brazing has been defined by the American Welding Society as "a group of welding processes wherein coalescence is produced by heating to a suitable temperature above 420°C (800°F) and by using a nonferrous filler metal, having a melting point below that of the base metals. The filler metal is distributed between the closely fitted surfaces of the joint by capillary attraction."

Soldering is defined as the use of a relatively low melting point alloy to unite metals of a higher melting point; soft solders are usually lead-base alloys whereas hard solders are generally copper-base or gold-base alloys.

Glass seals are not considered suitable for sealing large hybrid packages but are acceptable and commonly used for package sizes smaller than 1 inch x 1 inch. A typical example of glass sealed packages is the ceramic DIP package frequently employed to provide a hermetic seal for monolithic integrated circuit devices. In this case, glass frit is used to seal a metal or ceramic lid to the ceramic base.

3.2.2 Large package sealing and resealing methods. In general, larger packages (dimensions larger than 1 inch x 1 inch) are more difficult to seal than smaller ones. The hermeticity yield decreases as the size of the package increases.

One of the major findings of a recent RADC sponsored study[1] on sealing large, empty packages was that one of the weaknesses of this sealing was the rework capability; very few of the soldered or welded package types could be reworked with any degree of confidence, regardless of the method employed in sealing them. It was also determined in the course of this study that certain sealing methods, such as peripheral soldering and thermal conductivity soldering (using 80 Au/20 Sn preforms) presented more delidding problems than, for example, soldering using manual techniques and lower melting point solder alloys.

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[1] P. F. Manno, "Evaluation of Techniques for Sealing Large Hybrid Packages," GOMAC 1976, pp. 144-147, Orlando, Florida.

The sealing methods employed in the RADC program were:

(a) Parallel seam welding.

(b) Parallel seam soldering (80 Au/20 Sn) alloy).

(c) Peripheral soldering (80 Au/20 Sn).

(d) Thermal conductivity (gradient) soldering (80 Au/20 Sn alloy).

(e) Manual soldering (Sn 10 solder alloy) using a soldering iron.

A. Environmental Testing Results. Of the 183 packages tested, 96 percent (174) passed the entire array of environmental tests without a failure of the seal between the cover and the package.

In this group, failures of resealed packages are broken down as follows:

(a) 75 packages of all types were submitted to salt atmosphere, 150°C storage and 200°C storage.

Twelve of the 75 packages were subjected to resealing. Five of the twelve resealed packages failed leak test, of which one soldered and one welded package leaked due to failure of the lid-package seal during +200°C storage and during salt exposure. The remaining three leakers were due to failure of the glass-pin seal during +150°C and +200°C storage for 1000 hours.

(b) 108 packages of all types were submitted to seven other environmental tests. Of the 13 resealed packages utilized, only one failed; this was a seam welded package with a leak (at the pins) detected after acceleration testing.

B. Acceptance and Special Test Results. Although there is poor correlation between PIND test and radiographic examination for detection of particles, the x-ray method is still considered to be a very useful technique for detecting the following defects in soldered packages:

(a) voids in the solder flow along the sealing perimeter

(b) incomplete solder wetting along the peripheral seal area

(c) excessive solder flow inside the package.

The PIND test results indicated that the resealed, seam welded metal butterfly packages provided by one vendor had no metal particles generated by the welding process.[1] Specifically, these packages had 100 percent sealing and resealing yields. Nineteen of these packages were seam welded and all nineteen were non-leakers. Of these nineteen, new covers were resealed to seven and all seven were non-leakers.

Based on post resealing, PIND and leak test results, the performance of the reworked, seam soldered metal-glass butterfly packages supplied by one vendor were comparable to that of reworked, seam welded metal platform packages obtained from a different vendor.

C. Other Sealing/Resealing Studies. An aerospace division of the General Electric Company published an informative paper[2] in 1975 on the subject of repairs to complex hybrid circuits. Although no detailed information was presented regarding package types, sealing methods and sealing equipment used, it was stated that this investigation consisted of:

(a) Five different designs covering both digital and linear type circuits,

(b) Each circuit had a thin film substrate with a minimum of eight deposited (thin film) resistors,

(c) Each substrate contained silicon IC's, transistors and diodes in various quantities,

(d) The average number of wire bonds per circuit assembly was greater than 200,

(e) The end use was a digital subsystem used in a space application,

(f) All circuits were assembled in the same manner: thin film substrates were utilized with the semiconductor chips attached by eutectic bonding or with a non-conducting organic material and gold wire ultrasonic bonding was used for the interconnections,

(g) All packages were either solder sealed or weld sealed.

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[2] A.P. Bertin and T.W. Terwilliger, "Repairs to Complex Hybrid Circuits - Their Effect on Reliability," IEEE Rel. Physics Symp., Las Vegas, 1975, pp. 242-247.

The salient findings of this study were as follows:

(a) Each resealing process had specific problems associated with it.

(b) Although the removal of a soldered cover does not create a particular problem associated with high heat, the inability to remove all the solder at the seal location is a source of concern; the reason is that for an opened, solder sealed package, the high temperature associated with die replacement causes the remaining solder to become fluid and mobile. To ensure that the solder did not drop on a gold substrate conductor run, or form a mobile solder ball, it was determined that the reinspection of this repair had to be performed carefully.

(c) It was found that the removal of a cover attached by welding was more difficult to perform; this could result in many metal particles being formed and dispersed inside the package. It was necessary to develop a special (unspecified) cleaning process and to add a visual inspection.

(d) It was determined that two reseals (solder or weld) were not harmful when performed in a controlled manner. There was no apparent incompatibility between two reseals (solder or weld type) and the use of epoxy mounted substrates.

Additional information on the resealing of soft solder sealed packages has been provided by an earlier evaluation[3] conducted by Hughes Aircraft. Tests were carried out using 1 inch x 1 inch and 1 inch x 2 inches ceramic base packages, containing complex hybrid microcircuits and sealed with metal (Kovar) lids using Sn63 and Sn96 solder alloys. Delidding was accomplished by inverting the hybrid, with the lid down, on a hot plate, which permitted easy separation of the package as soon as the solder melted.

A study[3] was also conducted on the number of times a package could be solder sealed. It was established that the packages could be successfully

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[3] J.H. Holley, "Solder Sealing of Large Hybrid Microcircuits," Proceedings of 1970 Electronic Components Conference, May 1970, pp. 5-11.

delidded and resealed as many as four times. The number of times a unit could be sealed was a function of the thickness of the nickel coating over the molybdenum-manganese metallization layer. During the tinning operation and during the first seal, the outer gold layer is completely dissolved by the solder, which places the nickel in direct contact with the solder. After all the nickel is dissolved by the solder, the latter does not bond to the molybdenum-manganese surface. A nickel film thickness of 200 to 250 micro-inches permits in excess of 4 to 5 sealing cycles when using the Sn96 solder.

Temperature excursion of the active devices did not exceed 57°C during the sealing operation. The maximum temperature on the face of the substrate during sealing was 80°C. During the delidding process, the active devices reached a maximum temperature of 127°C; the substrate temperature was 135°C. It should be noted that only slightly higher substrate temperatures were obtained in the RADC sponsored study[1] which used a higher melting point alloy (Sn 10, M.P. = 299°C).

(a) Maximum substrate temperature during sealing was 138°C.

(b) Maximum substrate temperature during delidding was 199°C. For the most part, however, the solder sealing/delidding process does not require excessively long times or produce high temperatures (>250°C) that would degrade the materials inside the package. It should be emphasized, however, that other sealing techniques produce very high temperatures, which could initiate degradation of materials and wire bonds within the hybrid package, if excessive thermal exposure times are used during lid removal; for example, in the delidding tests[1] performed in the RADC study on five package types, one of the metal package types and two of the ceramic-based package types all reached delidding temperatures of 290°C to 374°C, as measured by a thermocouple mounted in a corner of the package during the reflow of the 80 percent gold/20 percent tin solder alloy. (See Table 1.)

TABLE 1. EFFECT OF DELIDDING METHODS ON HYBRID MICROCIRCUIT RELIABILITY

	POTENTIAL RELIABILITY IMPACT			DELIDDING PROCESS HAZARD RATING
METHOD OF LID REMOVAL	CHEMICAL CORROSION	THERMAL	MECHANICAL	
I. HEAT SOLDERING IRON HOT PLATE SOLDER POT FURNACE HEAT GUN	FLUX, FLUX REMOVER, EPOXY OUTGAS PRODUCT	SOLDER SPLATTER, CHIP DIFFUSION, BOND-PAD OXIDATION, EPOXY CHARRING, RESISTOR DRIFT	SOLDER BALLS SOLDER EMBRITTLEMENT, SOLDER LEACHING, GLASS BEAD CRACKS, COMPONENT OR SUBSTRATE CHIP/CRACK	VERY HIGH
II. ABRASIVE SAND FILE GRIND	GRIT CLEANING SOLVENTS, METAL FLAKES, UNPLATED BASE METAL	NONE	VIBRATION DAMAGE (CRACKS, CHIPS), GRIT IMBEDMENT (PARTICLES), CLAMPING AND HANDLING STRESSES	HIGH
III. MACHINE MILL SAWCUT ENGRAVE	CUTTING COOLANTS, SOLVENTS; METAL FLAKES, UNPLATED BASE METAL (OXIDATION)	NOT PROBABLE	CLAMPING AND HANDLING STRESSES, VIBRATION DAMAGE TO WIRES, SUBSTRATES, CHIPS, GLASS BEADS.	HIGH
IV. OTHER LASER E-BEAM PRY UP (HAND) ETCH	METAL FLAKES, CLEANING SOLVENTS ETCHANT RESIDUE	METAL SPLATTER	GLASS BEAD STRESSES; CLAMPING STRESSES, SNAP-OFF SHOCK	HIGH

A more recent evaluation of seam-welded packages has been carried out by Fancher and McDaniel.[4] This study was conducted to determine the effect of package variables on sealing, to optimize the welding process parameters, to develop efficient package rework techniques and to establish visual and mechanical inspection criteria.

Assessment of seal integrity and materials compatibility was achieved using environmental exposure, destructive analysis and nondestructive testing of two sizes of plug-in style metal packages. Plug-in style packages were selected for ease of sealing and to accommodate flow soldering for attachment to printed circuit boards.

[4] D.R. Fancher and J.E. McDaniel, "Seal and Rework Evaluation of Seam Welded Hybrid Packages," Electronic Packaging and Production, February 1978, pp. 89-94.

Plated finishes on the Kovar bases and Kovar covers were representative of those available in the industry. Nickel and gold-plated Kovar covers were selected for welding to nickel-plated bases, gold-plated bases and unplated Kovar bases.

The major findings of this study[4] were as follows:

(a) Provided the cover-to-base fit is satisfactory, parallel seal welding of plug-in type packages is not sensitive to power, travel and dwell settings of the machine, within broad limits.

(b) The cover-to-base plating combinations were ranked according to overall effectiveness: gold-to-gold, gold-to-Kovar (rework), gold-to-nickel, nickel-to-nickel and nickel-to-Kovar.

(c) Rework techniques developed in this study provide a clean package interior and a weldable surface for resealing. Gold plated covers should be used for resealing to bare Kovar base surfaces. Packages with covers removed by milling have been resealed up to three times with no leak test failures. Particles were not introduced into the package during cover removal and reseal operations.

(d) Cover-to-header orientation must be controlled during sealing with less than 0.005 inch from cover edge to base edge maintained and less than 0.002 inch overlap of the cover beyond the base edge.

(e) Marginal sealing of packages can result in leak failures during environmental testing, which makes visual examination of seals for potential leak sites mandatory.

(f) Packages with excessive base-cover mismatch, pitted seals or evidence of insufficient corner welding should be rejected or rewelding should be attempted.

(g) Metallurgical cross-sectioning and mechanical pull testing of sealed packages provide adequate means for plating and seal examination. Material and process qualification can be accomplished by the use of mechanical pull testing to detect variations in seal integrity and plating adhesion. Gold welded to either gold or Kovar was characterized by a high pull strength and no weld interface failures (i.e., 100 percent cover fracture) whereas low strength welds were characteristic of all nickel plated surfaces (nickel-nickel, nickel-Kovar, nickel-gold).

3.2.3 Significance of results. Analysis of the data obtained from the literature survey indicates clearly that there is a rework problem associated with hybrid packages having dimensions greater than 1 inch x 1 inch. The basic problems are:

(a) removing the old solder-sealed cover quickly, without application of excessive heat,

(b) cleaning up the seal area on the old package without damaging the hybrid components,

(c) hermetically sealing a new cover to the old package without generating particulate contaminants.

The survey results[1,2,3] indicated, however, that if the package could be hermetically resealed, the resealed package would probably be just as good as the new package from the standpoint of its ability to withstand exposure to environmental testing. Test results showed that certain package types gave higher sealing yields when sealed by specific methods. The RADC test data,[1] for instance, showed that (a) seam welded (metal butterfly) packages from one vendor gave a 100 percent yield on both sealing and resealing, as determined by leak test criteria; (b) the resealing yield of the seam soldered and seam welded packages from two other vendors was less, but was still rated good.

The following are procedures for the delidding of packages:

A. Removal of soldered lids.

1. Soft solder sealed. A temperature in excess of 299°C is required to remove a lid which has been soldered with Sn 10 (M.P. = 299°C); this can damage the polymeric (epoxy) adhesives or sensitive active device chips if the dwell time is too long. On the other hand, a too-fast rise time to flow the soldered lid seal may lead to cracking of ceramic substrates or glass seals due to thermal shock. Careful control of the temperature is a critical requirement of the delidding process.

A commonly used method is to invert the package and lower it into a solder pot until the molten solder just comes into contact with the lid. The temperature of the molten solder in the pot should be just high enough to melt the solder seal in about a minute or less. This technique allows good control of the package temperature and minimizes the probability of the formation of solder balls and splatter; it also diminishes the probability of thermally damaging sensitive components. To further minimize shock damage, packages to be delidded can be preheated to an intermediate temperature (100° - 150°C) prior to use of the solder pot.

2. Hard solder sealed. For packages sealed using a higher melting point hard solder, such as 80 percent gold/20 percent tin, lid removal can be accomplished using either thermal or mechanical methods.

If a mechanical method is to be employed, it is recommended that the hard soldered flat lid be removed carefully by peeling the lid up. The package is held in a clamp without damaging the package. A sharp blade is then inserted under a corner of the lid at a point near the side wall, and the lid is carefully peeled back. This method, although considered to be relatively benign, subjects the hybrid to mechanical stresses and may introduce metal flakes into the package.

B. Removal of welded lids. Welded lids can be removed by one of several methods, such as abrasive, machining, laser cut, electron beam cut or manual (pry-up) techniques.

It is recommended, however, that welded lids be removed by special machining methods, such as using a special edge milling technique.[4]

This milling machine method has proven to be very successful in delidding without damage. Although it is dependent on the skill of the operator, the application of careful technique during the machining of the lid surface virtually eliminates the introduction of metal particles into the hybrid package. Other machining methods, such as engraving and high speed sawing, were also evaluated in the course of development of this machining method. Particulate contamination by metal flakes and vibrational stress damage were the major problems encountered with the other two delidding methods.

The machine is adjusted to cut only the cover edge and welded area to the top surface of the package base. Cutter location is controlled by forcing the package against a stop adjacent to the cutter and moving the part along the stop. During the cutting operation, the packages are held inverted and since the lids remain intact, particles are not introduced into the package. A vacuum line may be attached near the cutting surface to insure particle removal. Precautions should be taken to prevent application of excessive clamping force on the package during cover removal.

Resealing of the packages, after rework of the defective hybrid components, may commence after the package base surfaces have been dressed flat using one of the following resurfacing operations:

C. <u>Package resealing by soldering (soft solder)</u>.

(a) Solder remaining on the package base must be resurfaced by reflow of the solder in the presence of flux, if required. Excess solder should be removed by an appropriate solder wicking technique.

(b) Flux residues must be removed carefully from the sealing surface using methyl alcohol (alcohol or flux must not flow inside the package) or other compatible solvent. The cleaning process must be qualified before use.

(c) Any loose particulate matter must be removed (mechanically or by cleaning in Freon TF vapor).

(d) A visual inspection must be performed after cleaning, to insure that all particulate matter has been removed prior to resealing.

It is recommended that tinned Kovar bases be limited to resoldering not more than four times, provided the original nickel film thickness is at least 200-250 microinches. After sealing with a new lid, hermeticity of the soldered seal would be checked using fine and gross leak tests.

Hybrids for all military and space applications should be subjected to the following additional acceptance tests after rework:

(a) PIND testing, to detect particles not removed by the cleaning process or metallic debris generated during the sealing process.

(b) Radiographic examination by x-rays, to detect voids or incomplete wetting by solder in the sealing perimeter. The x-rays may also detect a high percentage of larger particles of high atomic number metals or alloys (e.g., lead, tin, gold and Kovar). The x-ray method for particle detection can be improved by performing a PIND test between two consecutive radiographic examinations.

It is recommended that leak tests and PIND tests be made on a 100 percent basis for space grade and Class B hybrids. Radiographic examination may be considered as an adjunct to the PIND test, but is not considered to be a sensitive technique for particle detection, as shown by various studies.[1]

D. Package resealing by welding. The use of a benign delidding process, equivalent to that obtained by application of good technique and a properly designed delidding machine, does not normally introduce particles inside the hybrid package. Resurfacing of the package sealing surface, however, presents a reliability hazard since the preferred dressing technique is abrasion, to form a new, flat surface suitable for welding.

After resurfacing the package sealing surface and upon completion of the necessary circuit rework, the hybrid should be cleaned thoroughly. An internal visual inspection should be performed immediately prior to resealing, using a stereomicroscope, according to MIL-STD-883B (Method 2017.1).

E. Package resealing by soldering (hard solder). It is possible that thermal damage to hybrid components may occur during the solder reflow delidding process, which can produce package temperatures up to 315°C during the delidding of ceramic base packages.

The removal of the lid by thermal or mechanical means creates another problem: the remaining surface (the hard solder alloy) must be dressed flat by grinding, milling, etc., to permit another preform to be used. Probability of generation of metal particles during the dressing step is rated very high. It is recommended that after resurfacing of the hard solder alloy, the inverted package be cleaned followed by a thorough visual inspection for particles.

As shown in the RADC study, except for the metal butterfly packages from one vendor, the resealing hermeticity yield of packages sealed by 80 percent gold/20 percent tin (as determined by leak tests) was very low, in the range of zero to 57 percent yield.[1] The aforementioned results indicate that the resealing of packages using 80 percent gold/20 percent tin alloy solder is not a process that is easy to control and that there is a high degree of reliability risk associated with the delidding and resealing processes.

3.3 Task II - Eutectic attachment rework.

3.3.1 General. Active and passive chip components for hybrid microcircuits are attached to the substrate by various methods and materials. Typical attachment methods are:

(1) soldering

(2) eutectic alloy bonding

(3) bonding with polymeric materials, such as epoxy resins.

Similar processes and materials are also employed for the attachment of ceramic substrates to the package base. Polymeric attachment methods will be treated in Task III.

The term "eutectic bonding" refers to the use of a minimum melting point alloy consisting of two or more metals. A eutectic alloy changes (at the eutectic temperature) directly from a solid to a liquid, whereas a non-eutectic alloy passes through a "plastic" stage, from a solid to a liquid, over a wide temperature range. Fluxes are normally not used with eutectic bonding of components in hybrid microcircuit. The eutectic alloys commonly used for die attachment are Au-Ge and Au-Si. Other non-eutectic alloys are occasionally used, sometimes with dice attached (by eutectic bonding) to molybdenum or tungsten tabs; these include some of the lead-tin alloys or even the indium compositions.

Component attachment using alloys generally requires that both surfaces to be bonded be metal. In the case of eutectic alloy bonding of silicon devices, such as power, field effect and small signal transistor chips, a thin film of gold backing is generally provided as standard by the manufacturer, whereas integrated circuit chips are not normally furnished with metallized backing. The gold backing facilitates formation of the Au-Si eutectic alloy. A backing of chromium-silver is often used when solder preforms are used to metallurgically attach power transistor chips to a metal tab (or to a substrate) using a solder alloy, such as 92.5 Pb/2.5 Ag/5 In.

3.3.2 Active device eutectic and solder attachment methods. When hybrid microcircuit technology was in its infancy, active devices were either procured enclosed in standard packages or were eutectically bonded directly to the gold metallization of thick film substrates or to a gold plated molybdenum (or tungsten) tab in the case of thin film substrates. Passive devices, on the other hand, were usually bonded directly to the substrate conductor pattern using a low melting point alloy. During the hybrid assembly process, the pre-packaged active devices or chip-tab subassemblies were attached to the substrates using a low melting point solder. The use of low temperature solders for active device-metal tab attachment was dictated by the heat sensitivity of substrate-deposited thin film resistors. At that time, epoxy die bonding was not a reliable process.

Solder alloys can be deposited by various methods, ranging from a dip of the metallized substrate into a solder pot, to the more complex methods of deposition in vacuum by evaporation or sputtering techniques. The preferred methods, however, for placement of solder alloys for device bonding are (a) screened solder creams and (b) alloy preforms.

Face-up wire bonded active devices can be readily attached with solder alloys, but the choice of bonding alloy must consider the temperature excursions to be encountered during post die attachment processing.

Beam leaded devices can also be attached to a ceramic substrate by solder bonding techniques, if precautions are taken to prevent dissolution of the gold layer (of the beam) in the bonding alloy.(5)

(5) A.R. Kroehs, "Device - Substrate Bonding - Materials and Techniques." Electronic Packaging and Production, Vol. 10, No. 9, Sept. 1970, pp. 84-97.

Soldering of active and passive devices to substrates using solder flow/reflow techniques permits repairs to be made easily. Device replacement is usually accomplished without placing additional soldering alloy on the bonding pad.

Although hybrid circuit functional requirements and device attachment methods have changed considerably during the past decade and component density has significantly increased since the early days of hybrid technology, the need for eutectic bonding of active devices still exists. A metallic bond is always superior to other types of bonds, such as electrically conductive epoxy, when certain device requirements must be met, such as low thermal resistance, to reduce the thermal impedance between the device junction and the package case surface (R_{jc}). At 25°C, the thermal conductivity of an Au-Ge eutectic bond is 144 times higher than the conductivity of silver filled conductive epoxy.[6] The alloys commonly used to form a metallic bond with the bottom surface of active device chips are: 98 Au/2 Si (M. P. = 370°C); 88 Au/12 Ge (M. P. = 356°C); 95 Pb/5 Sn (M. P. = 310°C).[3] A list of die attach alloys, with compositions, melting points and applications, is presented in Table 2.[7] An excellent review of thermal design considerations for high power hybrids has been presented in a paper by Scapple and Keister.[6] This paper also illustrates possible methods for heat spreading when utilizing an alumina substrate, a molybdenum heat sink ("Molytab") or a copper heat sink, as shown in Figure 1.

An extensive evaluation of eutectic and solder bonding of active device chips has been reported by Himmel.[8] The overall objective of this study was to determine which die bonding process steps, if properly controlled, would reduce the formation of unsatisfactory metallic alloy bonds between

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(6) R. Y. Scapple, and F. Z. Keister, "A Simplified Approach to Hybrid Thermal Design," Solid State Tech., Oct. 1973, pp. 51-54, 62.

(7) C. E. T. White and H. C. Sohl, "Proforma on Preforms", Solid State Tech., Sept. 1975, pp. 45-48.

(8) Hybrid Microcircuit In-Process Qualification, Final Report, Aug. 1976, Contract No. ECOM-75-1311-F, R. P. Himmel, Hughes Aircraft Company, Culver City, CA.

TABLE 2. DIE ATTACH ALLOYS

ALLOY AND COMPOSITION (WEIGHT PERCENT)	TEMPERATURE, °C		DIE ATTACH APPLICATION
	LIQUIDUS	SOLIDUS	
58 Pb/40 SN/2Sb	231	185	GERMANIUM DEVICES
63.2 Pb/35 SN/1.8 Pb	243	185	GERMANIUM DEVICES
80 Aμ/20 SN	280	280	SILICON DEVICES
92.5 Pb/2.5 Ag/5 IN	300	–	SILICON DEVICES
97.5 Pb/1.5 Ag/1 SN	309	309	SILICON DEVICES
95 Pb/5 SN	314	310	SILICON DEVICES
88 Au/12Ge	356	356	SILICON DEVICES, GALLIUM ARSENIDE – PHOSPHIDE DEVICES
98 Au/2Si	800	370	SILICON DEVICES, GALLIUM ARSENIDE – PHOSPHIDE DEVICES
100 Au	1063	1063	SILICON DEVICES

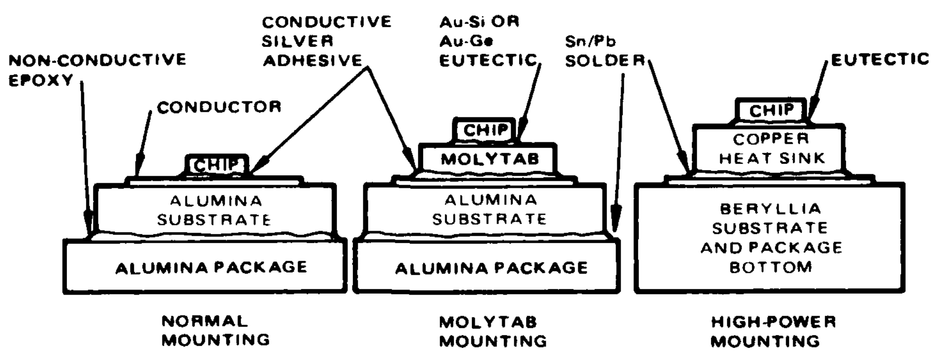

Figure 1. Possible methods for improving power dissipation.

silicon chips and either thin or thick film gold on alumina substrates. The relative importance of various processing equipment parameters, used during the bonding operation, were ascertained. Selected test techniques were utilized to determine which chip-to-substrate bonds were of satisfactory quality.

Selection of the metallic bonding systems was based on the material to be attached and the temperature required to provide good bonds. The gold-silicon eutectic alloy has been employed for many years to affix silicon chips to thick or thin film gold conductor layers by direct scrubbing of a bare (or gold plated) silicon chip to a gold conductor pad or by using a gold-silicon preform between chip and substrate. A list of the alloys used in the program are presented in Table 3. The other alloys used, gold-tin, Sn96, Sn62, and Sn60, do not alloy with silicon. In these cases, a barrier layer of either nickel or chromium, deposited on the bottom surface of the chip during device manufacture, provided the chip bonding surface. The bonding alloy preform or paste was placed between the chip and the substrate bonding pad metallization.

Table 4 lists the materials variables employed. Table 5 lists all the material combinations evaluated by Himmel.[8]

Various methods are available for metallurgically bonding active device chips to ceramic substrates. It has been claimed by Bull[9] that there are three basic techniques for this type of process, all of which utilize pulsed heat die bond methods:

(a) Electrode Current Heating

This method utilizes copper or tungsten tipped electrodes which contact the die pad. The equipment usually provides die pick up either manually or semi-automatically, whereby transfer of the chip to the chip pad is performed manually or automatically.

[9] D. N. Bull, "Advances in Low Temperature Bonding", Solid State Tech., Sept. 1974, pp. 60-65.

TABLE 3. EUTECTIC AND SOLDER ALLOYS USED TO ATTACH SEMICONDUCTOR CHIPS TO SUBSTRATES

ALLOY	COMPOSITION (BY WEIGHT)	MELTING POINT	
		°C	°F
GOLD/SILICON	94 Au · 6 Si	380	716
GOLD/TIN	80 Au · 20 Sn	280	536
Sn96	96 Sn 4 Ag	221	430
* Sn62	62 Sn 38 Pb	183	361
* Sn60	60 Sn 40 Pb	190	374

THESE TIN LEAD SOLDERS WERE USED BECAUSE OF FORM AVAILABILITY Sn62 PREFORMS AND Sn60 PASTE.

When the die and electrodes make contact with the chip pad, current flow commences from a constant voltage power supply and the temperature of the bonding pad around the chip increases. Concurrently, automatic scrubbing of the chip commences. The scrubbing operation, which can be controlled by time and amplitude, is effective in reducing voids. Bond quality is optimized by controlling three process variables: the electrode current, temperature of the workstage and temperature of the die collect. Careful selection of materials and process control can reduce the work stage temperatures to 200°C or less; actual work stage temperatures are highly dependent on the chip bonding pad material, however.

(b) Radiant Heating

This technique has been described in part during the review of the study conducted by Hughes.[8] A high wattage tungsten filament lamp is used to generate the pulsed heat, which is reflected and focused through an aperture in the work holder onto the back of the substrate. Apertures of various sizes are used, to match the different chip sizes. The die bonding pad is located directly over the aperture. Automatic mechanical scrubbing is started at a preset time after the lamp has been turned on, which permits the bonding pad to reach bonding temperature before scrubbing begins.

TABLE 4. MATERIALS USED FOR ACTIVE-DEVICE ATTACHMENT

USE	MATERIAL
DIE BONDING ALLOY	Au/Si, Au/Sn, Sn96, Sn60 OR Sn62. PREFORMS AND SOLDER PASTES WERE USED EXCEPT FOR Au/Si WHICH WAS ATTACHED BY EITHER DIRECT SCRUBBING OR A PREFORM.
PREPARATION OF CONTROL SAMPLES	NONCONDUCTIVE EPOXY – SCOTCHCAST 281. 1/ CONDUCTIVE EPOXY – ABLEFILM 606-2. 2/
DIE BACKING MATERIALS	NONE, GOLD, GOLD-OVER-CHROMIUM, SILVER-OVER-CHROMIUM.
SUBSTRATE METALLIZATIONS	THIN-FILM: NICHROME-NICKEL-GOLD ON 99 PERCENT Al_2O_3. THICK-FILM (ALL ON 96 PERCENT Al_2O_3): (1) ESL 8835 GOLD 3/ (2) ESL 8835 GOLD OVER ESL 5800B PLATINUM-GOLD (3) EO 06990-S GOLD. 4/ (4) EO 06990-S GOLD OVER ESL 5800B PLATINUM-GOLD.

1/ SCOTCHCAST = 3M, 6411 RANDOLPH STREET, LOS ANGELES, CA.

2/ ABLEFILM = ABLESTICK ADHESIVE CO., 833 W. 182ND ST., GARDENA CA 90247.

3/ ESL = ELECTRO-SCIENCE LABORATORIES, 1601 SHERMAN AVENUE, PENNSAUKEN, N.J. 08110

4/ EO = ELECTRO OXIDE CORP., 3896 BURNS RD., PALM BEACH GARDENS, FLORIDA 33410

TABLE 5. MATRIX SHOWING THE MATERIALS AND PROCESSES USED IN THE FABRICATION OF THE SPECIMENS FOR TESTING ATTACHMENT OF ACTIVE DEVICES (I. E., SEMICONDUCTOR CHIPS). THE BLOCKS MARKED BY X REPRESENT COMBINATIONS WHICH WERE EVALUATED

			THIN FILM SUBSTRATE				THICK FILM SUBSTRATE																	
FILM METALLIZATION			GOLD OVER NICKEL OVER NICHROME				FRITTED GOLD INK				FRITLESS GOLD INK				FRITTED GOLD OVER PLATINUM GOLD INK				FRITLESS GOLD OVER PLATINUM GOLD INK				PLATINUM GOLD INK	
CHIP BACK METALLIZATION			NONE	AU	AG/CR	AU/CR	NONE	AU	AG/CR	AU/CR	NONE	AU	AG/CR	AU/CR	NONE	AU	AG/CR	AU/CR	NONE	AU	AG/CR	AU/CR	AG/CR	AU/CR
METHOD OF BONDING CHIP TO SUBSTRATE	AU-SI EUTECTIC	DIRECT SCRUB	X	X			X	X			X	X			X	X			X	X				
		PRE FORM	X	X			X	X			X	X			X	X			X	X				
	AU-SN EUTECTIC	SOLDER PASTE				X				X				X				X				X		
		PRE FORM				X				X				X				X				X		
	SN 96 SOLDER	SOLDER PASTE				X			X	X			X	X									X	X
		PRE FORM				X			X	X			X	X										
	LOW TEMP SOLDER	SN 62 SOLDER PASTE				X				X				X										X
		SN 60 PRE FORM				X				X				X										
	NON CONDUCTIVE EPOXY	PASTE		X																				
	CONDUCTIVE SILVER EPOXY	PASTE		X																				

Work stage temperatures for radiant heating type equipment are usually in the 270° - 320°C range.

(c) Hot Gas Bonding

The hot gas bonding method employs a hot gas jet to heat the die pad to the bonding temperature. The jet is positioned such that, as the die collet approaches the die pad, the movement of the collet is interrupted, and the gas, usually nitrogen at a temperature in excess of 500°C, is impinged onto the pad. The chip is brought to the bonding pad after several seconds, at which time automatic (or manual) scrubbing and timing begins. Optimization of the bonding process is achieved by control of the work stage and collet temperature.

Work stage temperature requirements depend on the die size and the gas jet temperature. For small chips, temperatures as low as 150°C have been employed, but typically, stage temperatures will fall in the range 300°C - 320°C.

Although it has been reported that the hot gas does not affect electrical parameters of the active device chip, it is recommended that this factor be evaluated for each chip type to be used in a microcircuit.

It should be noted that all commercial types of pulsed heat die bonders are equipped with nitrogen cover gas to prevent bonding alloy oxidation; these bonding machines are also usually equipped with a nitrogen cooling jet, which automatically turns on after the bonding operation ceases and further reduces the effect of heat on the chip's electrical parameters.

3.3.3 Significance of results.

3.3.3.1 Materials and processes. The following conclusions are based on the literature active-device-attachment evaluation:[8]

- The most significant machine variables were collet temperature and substrate temperature. Scrub time had a noticeable effect.

- Collet load, tool-down time, and protective atmosphere (N_2) flow rate were the least significant bonding machine parameters. The protective atmosphere serves to keep particles out.

- Of the material combinations, the interface alloy appeared to have the most significant impact on the resultant die bond. This was somewhat more noticeable than chip backing and substrate metallization effects.

- Device attachment to the thin-film metallization of gold-over-nickel-over-nichrome gave better results than any of the fritted or fritless thick-film gold metallizations.

- The use of platinum-gold ink beneath the gold ink gave better die attach results than the gold ink alone.

- Good bonds could be obtained using the Au/Si and Au/Sn alloys, but the Sn96, Sn62, and Sn60 solders all yielded unsatisfactory die bonds. The Au/Si eutectic provided the best die bond.

- Eutectic die bonding to thick-film gold on alumina must be done carefully to avoid the complete removal of conductive gold and the exposing of bare substrate.

- None of the control chips attached with either conductive silver epoxy or nonconductive epoxy failed any of the tests.

3.3.3.2 Qualification testing. The following conclusions are based on in-process testing used to evaluate the various combinations of die-attach materials.[(8)]

- Close visual inspection is the most reliable active-device bonding evaluation technique.

- Mechanical shock testing or push-off testing are of value in evaluating process reliability.

Solder voids can often be detected beneath the chip by non-destructive electrical measurements. Power transistors, for instance, usually involve a metallurgical bond to the collector. According to Johnson[10], forward-biased second breakdown is critically dependent on the dynamic thermal impedance, and impediments to the diffusion length can be readily detected.[11] Power test evaluation can be non-destructive if the circuit has an adequate crowbar protection.

3.3.4 Passive device attachment using metallurgical processes. Present day military grade hybrid microcircuits differ in their construction details between the various manufacturers, but all incorporate passive components of various sizes and types. The passive elements are generally chip type devices, but occasionally, discrete miniature components are utilized when the desired part is not available in chip form.

Capacitors, resistors and inductive devices are all currently available in chip form. Attachment of the chip devices may be readily accomplished using metal alloys, conductive epoxy or non-conductive epoxy. Ceramic chip capacitors and thick film chip resistors, for example, can be fabricated with metallized terminations, which facilitates attachment to the substrate using conductive epoxy or reflow solder techniques.

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(10) J. E. Johnson, "Die Bond Failure Modes", IEEE Rel. Physics Symp., April 2-4, 1974, pp. 150-154.

(11) P. L. Hower and P. K. Govil, Tech. Digest, I. E. D. M., Washington, D. C., p. 335, 1973.

(12) Electronic News, Nov. 27, 1978, p. 22.

In the present review of the literature on rework of eutectically attached passive devices, chip capacitors have been selected for study because they fairly represent other types of passive chip devices, such as chip resistors, due to the presence of different materials both in the chip-to-substrate bond and in the capacitor body itself. Ceramic chip capacitors, as represented by the NPO and the K series types, are very popular for hybrid applications due to their favorable costs, superior electrical characteristics, ease of replacement, convenience in processing and substrate space efficiency.

Although both solder and epoxy bonding of capacitors has been evaluated in depth in one reference,[14] the objective of the present literature review is to evaluate the rework aspects of alloy bonded chip capacitors and substrates.

Failure of ceramic chip capacitor interconnections is caused chiefly by the difference in thermal coefficients of expansion between the capacitor body and the ceramic of the substrate.[13] One type of barium titanate capacitor (K1200) has a nominal thermal expansion coefficient of $12.5 \times 10^{-6}/^{o}C$, which is two times larger than the ($6.3 \times 10^{-6}/^{o}C$) coefficient for alumina.

In an evaluation[14] of the effect of various design factors on passive device attachment reliability, ceramic chip capacitors were studied exclusively. For a variety of size and material conditions, three capacitor sizes with three different end metallization systems were employed. The capacitor chips were either soldered or epoxy bonded to thin or thick film metallization or alumina substrates. A list of materials and processes used is presented in Table 6.

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(13) G. A. Dreyer, A. Koydounaris and I. H. Pratt, "The Reliability of Soldered or Epoxy Bonded Chip Capacitor Interconnections on Hybrids," IEEE Trans. on Parts, Hybrids and Packaging, Vol. PHP-13, No. 3, Sept. 1977.

(14) R. P. Himmel, Hybrid Microcircuit In-Process Qualification, Final Report, August 1976, ECOM-75-1311-F, Hughes Aircraft Company, Culver City, CA.

TABLE 6. COMPONENTS AND MATERIALS EVALUATED IN THE CAPACITOR TEST PROGRAM

COMPONENT	DESCRIPTION
CAPACITOR SIZES (CAPACITORS WERE TYPE K1200, PURCHASED FROM U.S. CAPACITOR CORP)	SMALL (0.050-INCH x 0.080-INCH x 0.050-INCH HIGH) (1.27 x 2.03 x 1.27 MM)
	MEDIUM (0.080-INCH x 0.180-INCH x 0.050-INCH) (2.03 x 4.57 x 1.27 MM)
	LARGE (0.080-INCH x 0.270-INCH x 0.050-INCH (2.03 x 6.86 x 1.27 MM)
CAPACITOR END TERMINATIONS	SILVER
	PALLADIUM-SILVER
	COATED WITH A SOLDER ALLOY OF Sn60/Pb36/Ag4
CAPACITOR INTERCONNECT METHOD	REFLOW SOLDERING OF Sn10 AND Sn96 TINNED PADS
	REFLOW SOLDERING OF Sn62 SOLDER PASTE
	CONDUCTIVE SILVER EPOXY (CURED AT 125°C FOR 2 HOURS) = ABLESTIK NO. 606-2
	NONCONDUCTIVE EPOXY (CURED AT 125°C FOR 2 HOURS) WITH INTERCONNECTIONS MADE WITH 0.002-INCH – (50.8 μM) DIAMETER THERMOCOMPRESSION BONDED WIRE. THE WIRE BONDS WERE NON-DESTRUCTIVELY PULL TESTED AT 3 GRAMS. (SCOTCHCAST NO. 281)
SUBSTRATE TYPE	THIN-FILM. 99 PERCENT ALUMINA WITH EVAPORATED NiCr/EVAPORATED Ni/PLATED Au
	THICK-FILM. 96 PERCENT ALUMINA WITH ESL 5800B PLATINUM-GOLD

The capacitor interconnect configurations are shown in Figure 2.

Epoxy bonded capacitors were attached using either conductive or non-conductive materials, which were cured at 125°C for two hours in a circulating air oven. Both types of epoxy adhesives were applied manually, using the end of a plastic toothpick.

Different size conductor pads (small, medium and large) were utilized to determine if the pad size had a significant effect on incidence of chip failures.

As shown in Figure 2, those capacitors which were bonded with conductive epoxy to thick film conductors were also attached at their midsections with non-conductive epoxy. The capacitors which were attached completely with non-conductive epoxy were connected electrically to thick or thin film conductors using (thermocompression) gold wire bonds, whereas those that were attached to thin film substrates using conductive epoxy were not attached at their midsections with nonconductive epoxy.

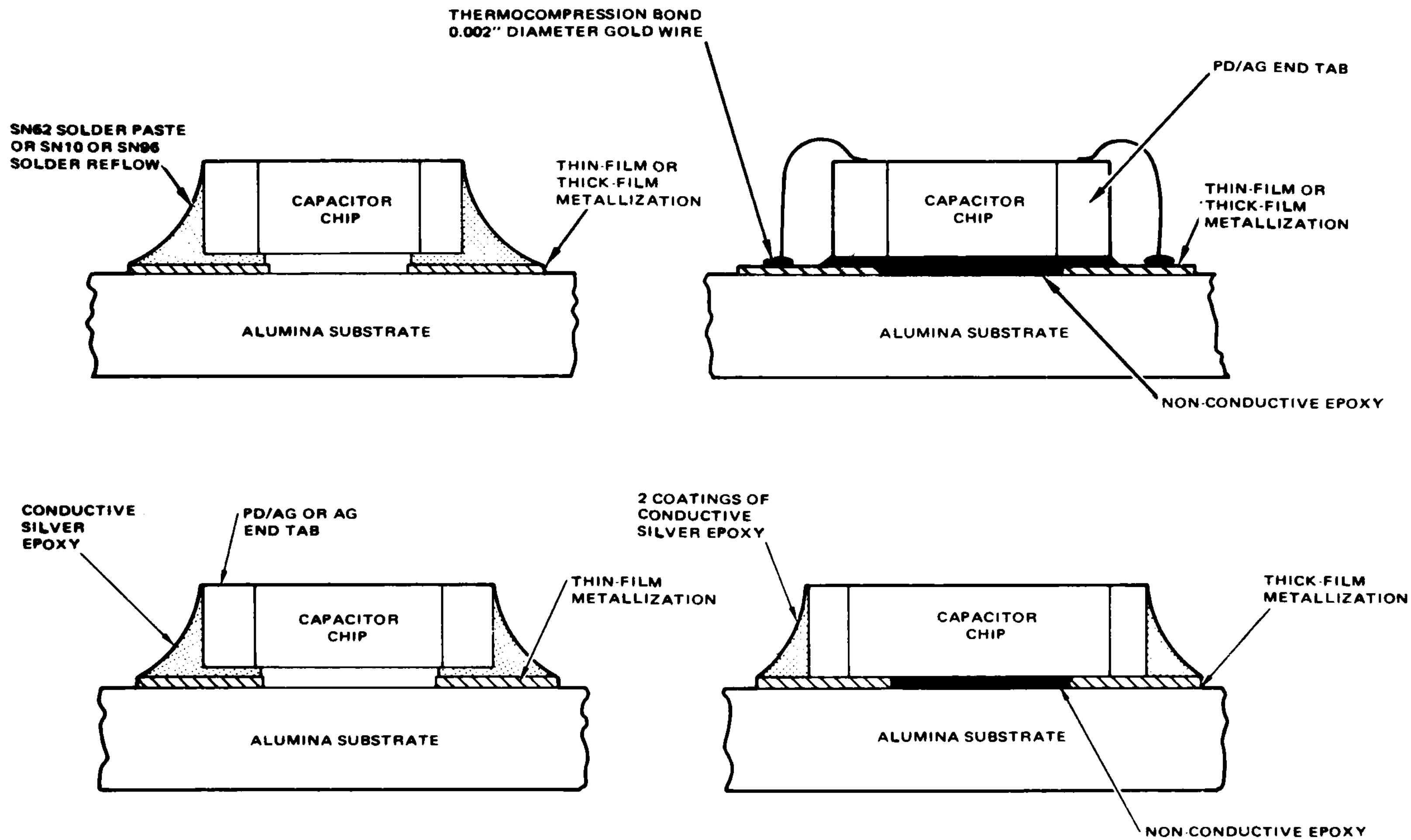

Figure 2. Capacitor chip interconnection configurations.

After assembly, all specimens were subjected to a group of environmental tests, (as shown in Figure 3) consisting of: mechanical shock, temperature cycling, mechanical shock and high temperature storage.

After each environmental test, the specimens were examined visually and electrically tested for any component changes. An electrical failure was defined as (a) an electrical "open" circuit or (b) a change of 10 percent or more in capacitance. Mechanical failures were reported if any cracks or separations appeared between capacitors and substrates.

Test results are summarized in Table 7.

The results of the chip capacitor evaluation have been summarized as follows:

3.3.5 <u>Significance of results.</u>

3.3.5.1 Materials and processes. The overall reliability ranking of the methods of attachment evaluated were:[14]

(a) Sn10 solder

(b) Non-conductive epoxy with 0.002 (50.8 μm) inch gold wire TC interconnects

(c) Sn62 solder

(d) Sn96 solder

(e) Silver-filled conductive epoxy.

The following conclusions may be drawn from this evaluation:[14]

- Capacitors were less likely to fail electrically or mechanically when bonded to thick-film metallization than when bonded to thin-film metallization.
- Chips were less likely to fail when bonded to large pads than when bonded to medium or small pads. Surprisingly, bonding to medium pads was apparently slightly less reliable than bonding to small pads.
- For soldered capacitors, the capacitor end termination electrical and mechanical reliability was, in decreasing order:

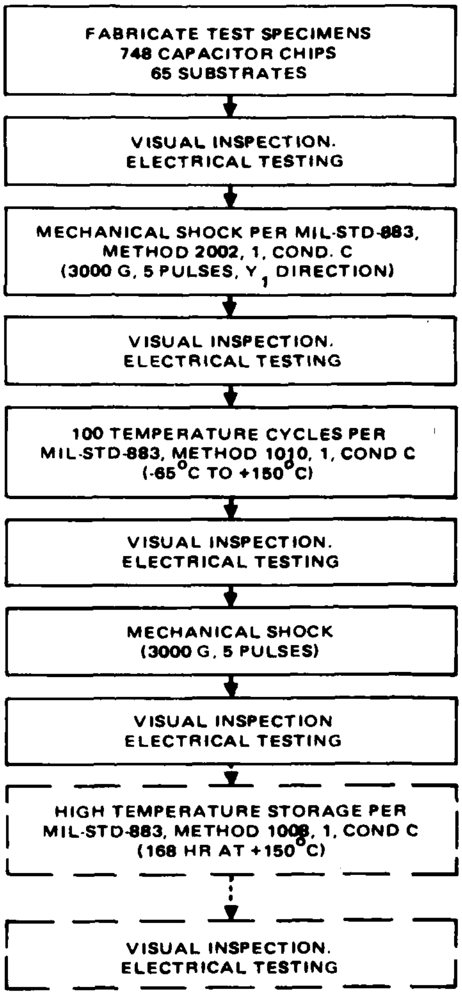

Figure 3. Block diagram flow chart for testing of capacitor chip attachment test specimens.

TABLE 7. EFFECT OF THE INTERCONNECT MATERIALS ON CAPACITOR BEHAVIOR

INTERCONNECT MATERIAL	ELECTRICAL FAILURES 1/				MECHANICAL FAILURES 1/				TOTAL REJECTS 3/	
	THICK FILM (F/T)	THIN FILM (F/T)	TOTAL (F/T)	% TOTAL FAILURES	THICK-FILM (F/T)	THIN-FILM (F/T)	TOTAL (F/T)	% TOTAL FAILURE	NUMBER (F/T)	%
Sn10	0/132	3/80	3/212	1.4	0/132	3/80	3/212	1.4	3/212	1.4
Sn96	4/132	18/80	22/212	10.4	1/132	9/80	10/212	4.7	23/212	10.8
Sn62	6/68	0/48	6/116	5.2	6/68	0/48	6/116	5.2	9/116	7.8
CONDUCTIVE EPOXY	3/92	6/52	9/144	11.9	43/92	31/52	74/144	51.5	74/144	51.5
GOLD WIRE AND NONCONDUCTIVE EPOXY 2/3/	1/24	2/24	3/48	6.2 2/	1/24	2/24	3/48	6.2 2/	3/48	6.2

1/ F/T – FAILURES/SAMPLE SIZE

2/ THERE WERE A TOTAL OF 3 WIRE BOND FAILURES ON THESE PARTS. THE BROKEN WIRES WERE MORE LIKELY DUE TO MISHANDLING RATHER THAN ENVIRONMENTAL STRESSES.

3/ THIS COLUMN IS NOT NECESSARILY THE SUM OF THE FIRST TWO COLUMNS BECAUSE SOME PARTS WERE BOTH MECHANICAL AND ELECTRICAL FAILURES.

(a) Pd/Ag end termination

(b) Solder or Ag end terminations

- For conductive-epoxy-bonded capacitors, the end termination electrical reliability was, in decreasing order:

  (a) Ag end termination

  (b) Solder end termination

  (c) Pd/Ag end termination

- For conductive-epoxy-bonded capacitors, the end termination mechanical reliability was, in decreasing order:

  (a) Pd/Ag

  (b) Ag

  (c) Solder

- The appearance of silver end terminations changed during environmental testing. The appearance of solder coated or Pd/Ag coated terminations was unaffected by environmental exposure.

- Soldered capacitors were more likely to fail electrically than mechanically.

- Conductive epoxy-bonded capacitors were more likely to fail mechanically than electrically.

- The larger the chip, the higher the probability of failure.

It should be noted that NASA recommends the use of epoxy for attachment of large chip capacitors.

3.3.5.2 Qualification testing. The relative severity of the environmental tests on electrical reliability was, in decreasing order:

(a) Mechanical shock

(b) Thermal cycle

(c) Mechanical shock (after thermal cycling)

(d) High-temperature exposure

The relative severity of the environmental tests on mechanical reliability was, in decreasing order:

(a) Mechanical shock after thermal cycle

(b) High-temperature exposure

(c) Thermal cycle

(d) Mechanical shock

Visual examination was of minimal value in detecting marginal capacitor chip attachments.

These conclusions essentially agree with those of Caruso,[15] Lasch,[16] and Olson,[17] who attributed most capacitor chip failures to a thermal expansion incompatibility. Caruso and Olson both found that temperature cycling, thermal shocks, and mechanical shocks (10,000 to 25,000 G) would produce capacitor chip failures.

3.3.6 Substrate attachment methods using metallurgical processes. Ceramic substrates are affixed to hybrid microcircuit packages using techniques and materials similar to those employed in attaching active and passive components to the substrate.

Although epoxy bonding of a substrate to the package base is a simple, reliable process, the use of eutectic (or alloy) bonding methods may be necessary, due to one or more of the following:

(a) the hybrid circuit may include one or more high power devices that require a high thermal conductivity path into the heatsink outside the package.

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(15) S. V. Caruso and J. O. Honeycutt, "Investigation of Discrete Component Chip Mounting Technology for Hybrid Microelectronic Circuits", NASA Tech. Memo TMX-64937, May 1975.

(16) K. B. Lasch and K. S. Lynch, 25th Proc. Electronic Components Conf., pp. 123-132, 1975.

(17) H. C. Olson, International Microelectronics Symp.), pp. 485-490, 1975.

(b) an all metal bonding system may be dictated because particular assembly processes, such as oven sealing, may preclude the use of organic materials in bonding the substrate to the package base.

Substrate attachment utilizing a metallic bond usually requires the use of an alloy having a higher melting point than that used for die attachment, if the chip bonding process (with an alloy) follows the substrate attachment process.

A significant reliability problem encountered in solder bonding of alumina substrates to package bases is the formation of voids at the package (metal or ceramic) - substrate interface. The "vacuum collapse" method of Bascom and Bitner[(18)] has been shown to be a very effective technique for essentially eliminating the thin films of entrapped air between soldered alumina plates. It was claimed that voids could be reduced from 50 percent of the bond area to less than 10 percent of the bond area.

Zimmerman[(19)] has studied the use of 78 Au/22 Sn as a hard solder for the attachment of substrates to hybrid packages, in place of the commonly used 80 Au/20 Sn alloy. The radiographic results of this study showed that the 78 weight percent gold alloy does not form the large voids, usually obtained with the 80 weight percent gold alloy, between the substrate and the gold plated kovar flat pack base. The mechanism postulated to be the cause of good wetting of the gold plated mating surfaces is based on the gold-tin phase diagram:

(a) the use of 80 Au/20 Sn alloy preforms causes the liquidus temperature to increase as gold enrichment (from the gold plated mating surface) of the liquid phase increases.

(b) the use of 78 Au/22 Sn preforms causes the liquidus temperature to decrease as gold enrichment of the liquid phase increases.

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(18) W. D. Bascom and J. L. Bitner, "Void Reduction in Large Area Bonding of IC Components", Solid State Tech., Sept. 1975, pp. 37-39.

(19) D. D. Zimmerman, "A New Gold-Tin Alloy Composition for Hermetic Package Sealing and Attachment of Hybrid Parts", Solid State Tech., January 1972, pp. 44-46.

Non-destructive examination of alloyed silicon chip-to-substrate bonds for voids can be performed by ultrasonic methods.[20, 21] The method, like sonar, depends on timing of ultrasonic pulse echoes. Scattering of the sonic pulse by the void decreases the echo signal level. This technique for detecting voids should be applicable to substrate - package metallurgical bonds.

A comparison of substrate attachment materials was performed by Koudounaris.[22] The objective of this task was to determine the relative merits of different adhesive materials used in the attachment of alumina substrates to ceramic and metal packages. The criterion employed was the strength of the substrate-package bond initially and after environmental tests.

Five attachment materials were evaluated:

(a) A conductive silver epoxy, Ablebond 606-2.

(b) A conductive silver epoxy, Ablebond 36-2.

(c) A non-conductive epoxy, Scotchcast 281.

(d) Sn62 solder (62 Sn/36 Pb/2 Ag, melting point 182°C).

(e) Gold/tin eutectic (80 Au/20 Sn, melting point 280°C).

Three package types were employed:

(a) A ceramic flatpack with metallized and unmetallized base.

(b) A metal platform-type package.

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(20) J. E. Johnson, "Die Bond Failure Modes", IEEE Rel. Physics Symposium, April 2-4, 1974, pp. 150-154.

(21) R. S. Gilmore, M. L. Torreno, G. J. Czernw and L. M. Burnet, "High Frequency Ultrasonic Testing of Bonds: Application of Silicon Power Devices", Materials Evaluation, January 1979, pp. 65-71 (Research Supplement.).

(22) A. Koudounaris, Hybrid Microcircuit In-Process Qualification, Final Report, October 1977, ECOM-76-1399-F, Hughes Aircraft Company, Culver City, CA.

After assembly, each 1 inch x 1 inch package was subjected to an environmental test sequence per MIL-STD-883 which included: 1500G mechanical shock, vibration test, temperature cycling, 3000G mechanical shock, followed by thermal shock. After each environmental test step, the packages were subjected to a PIND test to detect loose substrates and loose particles. At the conclusion of the environmental testing, the packages were delidded and visually inspected.

The test specimens were evaluated for (a) any evidence of loose substrate and (b) cracking or peeling of the attachment material. Any such evidence was considered to be a failure of the substrate-package bond.

According to these criteria, the best performance was obtained using Sn 62 solder, gold/tin eutectic alloy and Scotchcast 281 nonconductive epoxy. In fact, no failures were obtained with these three attachment materials. The packages fabricated with the two silver filled epoxies, on the other hand, produced a total of seven failures in a group of sixteen test specimens.

Thermal expansion differences did not appear to be a predominant factor affecting the substrate-package bond although the differences in expansion coefficients of the attachment materials and the package materials are large.

3.3.7 <u>Significance of results for metallurgically bonded active devices, passive devices and substrates</u>. The reworkability of an active or passive device attached to a substrate by a metallurgical bond is determined by several factors which have a significant effect on device reliability:

(a) Type of bond, alloyed versus non-alloyed. Gold-silicon forms a true alloyed bond to the base of a silicon chip, that is, silicon from the base of the chip has been dissolved by the Au/Si molten phase.

(b) Intermetallic compound formation.

(c) Leaching or scavenging of the conductor bonding pad metallization.

(d) Solderability.

Eutectic or alloy die bonding is most commonly used on (a) high power devices, such as diodes and transistors which require a very low ohmic contact and (b) non-passivated active devices that may be sensitive to contamination from organic materials, such as epoxies. A true alloy bond is formed between the silicon and the gold plated metal substrate, which is typically a refractory metal such as tungsten or molybdenum.

The silicon chip may also be attached directly to the thin film or thick film metallization on the ceramic substrate, using the Au/Si eutectic attachment process.

In the event the active device is thermally degraded at or above 400°C, a soldering process using a lower melting solder (e.g., 80 Au/20 Sn, 95 Pb/ 5 Sn) should be employed to bond the chip directly to the thick/thin film metallization of the ceramic substrate, to a refractory metal tab or to a metal heat sink. The bottom surface of the chip should be coated with gold, nickel or chromium to facilitate formation of a non-alloyed solder bond. Scavenging is the dissolution of the material from the surface to be bonded.[23] As an example, soldering of an active device chip to thick film substrate metallization pads using tin-rich solders usually results in dissolution of the thick film gold (or palladium-gold), leaving a glass rich surface under the bond or even the exposure of bare ceramic. It is recommended, therefore, that solders (for die attach) containing little or no tin be employed to permit die rework and the formation of a reliable reworked solder bond.

In the replacement of Pd/Ag terminated chip capacitors, scavenging or leaching is also a problem if the capacitors do not have a barrier layer.[24]

Intermetallic compounds also form in a layer at the termination-to solder (Ag or Pd/Ag - Sn60) interface whenever there is an elevated temperature exposure, such as during a 100 hour burn-in at 125°C.[24] The intermetallic compounds caused a decrease in part solderability and

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[23] S. S. Leven, <u>Solid State Tech.</u>, March 1977, pp. 39-41.

[24] G. J. Ewell, "Reliability Problems in Reflow Soldering of Ag and Pd/Ag Terminated Chip Components", 27th Electronic Components Conference, Arlington, VA. May 16-18, 1977, pp. 206-211.

appeared to cause a decrease in thermal shock resistance. Solderability decreased because the growth of the intermetallic layer, which consumes solder, both reduced the amount of solder available for reflow and elevated the reflow temperature by increasing the lead content of the remaining solder.

Studies conducted by Kinser and others[25] indicated that 63 Sn/37 Pb and 96 Sn/4 Ag reflow soldered chip capacitors (on thick film substrates) are not sufficiently reliable to be considered for use in high reliability space/ military systems. The cause of failure during thermal cycling appeared to be a strengthening of the solder by repeated strain during thermal cycling. The stronger solder does not deform as a virgin joint; therefore, the thermal expansion mismatch increased to levels at which joint failure occurred.

Active devices attached by hard solder are often under considerable stress and, in extreme cases, may fail by fracturing, but the hard solder alloy itself does not degrade by fatigue after many temperature cycles.[26] Soft solder die bonds, on the other hand, transmit very little stress to the active device chip, but undergo considerable degradation during temperature or power cycling by a process known as thermal fatigue, which is induced by the formation of intermetallic compounds. An investigation into the reliability of gold plating-solder attachments was recently conducted by Wright,[27] who used eutectic solders of the Au-Ge, Au-Sn, Pb-Au and Sn-Pb-Ag systems in measuring the effect of solid state reactions upon the lap shear strength. It was shown that all five solders can be expected to exhibit adequate strength for microelectronic purposes for more than 10^5 hours at a sustained temperature equal to or less than 100°C, when the mating materials have similar coefficients of thermal expansion.

[25] D. L. Kinser, J. G. Vaughan and S. M. Graff, Electronic Packaging and Production, May 1976 (Nepcon '76 East Show Edition), pp. 61-68.

[26] D. R. Olsen and H. M. Berg, "Properties of Die Bond Alloys Relating to Thermal Fatigue," 27th Electronic Components Conference, Arlington, VA, May 16-18, 1977, pp. 193-198.

[27] C. Wright, "The Effect of Solid State Reactions Upon Solder Lap Shear Strength", 27th Electronic Components Conference, Arlington, VA, May 16-18, 1977, pp. 199-205.

Harman[28] has proposed the use of acoustic emission to screen the integrity of bonded capacitor chips in hybrids. Acoustic emission refers to the emission of broad band stress waves when materials are broken, cracked, or deformed. Test results on epoxy or solder bonded chip capacitors indicate that incompletely bonded capacitor chips can be detected using this technique.

A method of reducing voids in the metallurgical bonding of semiconductor devices to substrates (and substrates to ceramic bases) has been developed by Bascom and Bitner.[18] It is almost impossible to expect void-free bonds when using solder preforms to attach active device chips, such as large area integrated circuit chips, to alumina substrates. Thin films of air are almost always trapped at the chip-preform interface since the real area of contact between flat, rigid surfaces is usually 20 percent or less of the nominal contact area. It was demonstrated that a void content of 50 percent of the bond area can be reduced to less than 10 percent by performing the bonding under vacuum (2-3mm Hg, mechanical vacuum pump) but returning the system to atmospheric pressure while the solder is molten. Similar results were obtained in the bonding of thin film, gold plated alumina plates to each other.

3.4 Task III - Polymer (Epoxy) attachment rework.

3.4.1 General. The major advantage of using epoxy resins for attachment of devices to substrates, and substrates to packages, is the low processing temperatures. Curing cycles are typically a few hours at 120° - 150°C (in air). An important advantage of epoxy bonding techniques is that replacement of defective devices and substrates is facilitated.

A few of the drawbacks encountered in using epoxy are: (a) epoxy die attachment cannot be used for high power active devices, only for low to medium power devices; (b) very low ohmic contact requirements preclude the use of epoxy bonding; (c) epoxy has a higher electrical resistivity and

[28] G. C. Harman, "The Use of Acoustic Emission in a Test for Beam Lead, TAB, and Hybrid Chip Capacitor Bond Integrity", IEEE Trans. on Parts, Hybrids and Packaging, Vol. PHP-13, No. 2, June 1977, pp. 116-126.

lower thermal conductivity than metallic bonding materials; (d) epoxy may affect the electrical characteristics of unpassivated active and passive devices, due to outgassing of deleterious chemical species of the epoxy system; (e) epoxy outgassing may also contribute to the water vapor content of a hybrid package.

3.4.1.1 Device attachment techniques. Methods of epoxy application on hybrid circuits vary from manual placement using pointed applicators to automatic dispensers.[29] Epoxy dispensers are available from various equipment manufacturers which can be utilized for rework and small production quantities. Some of the problems which can be experienced with liquid dispensing systems for device attachment are: clogged capillaries, poorly controlled epoxy placement and variations in quantity dispensed. Another technique employed by some hybrid manufacturers is to screen print the epoxy paste in the proper size, shape and location for every die on the hybrid substrate. This technique permits deposition of a uniformly thick layer, typically 0.001 to 0.002 inch thick, (25.4 to 50.8 μm) on hundreds of substrates at a time. Since some epoxies may be stored for 2 or more weeks after printing, the epoxy coated substrates may be stored under clean conditions until ready for die assembly and curing.

3.4.2 Active device attachment processes. The process requirements for good epoxy die bonding are more subtle than those required for good eutectic bonds:[30]

(a) The die should be flat, the epoxy bond line thin and an epoxy fillet visible around most of the periphery of the die.

(b) There can be no epoxy build-up higher than the top surface of the die or shorting of the epoxy to wire bond pads on the die.

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(29) J. Kimball, "Epoxy Device Bonding and Handling Techniques for Hybrid Microcircuits", Solid State Tech., October 1973, pp. 55-58.

(30) D. N. Bull, "Advances in Low Temperature Die Bonding Techniques," Solid State Tech., pp. 60-65, Sept. 1974.

(c) If resin "bleed out" occurs, the wire bond pads on the substrate must be located far enough away to avoid any effect of the wire bond operation. Some resins produce lower "bleed out" than others.

The quantity of resin dispensed onto a substrate pad from the standard cartridge hypodermic needle type dispenser is controlled by the following variables:[30]

(a) Pressure into the cartridge

(b) Time of dispensing

(c) Size of the needle

(d) Position of needle above the pad

(e) Viscosity of the resin

Hybrid microcircuits usually contain chips of different sizes, which requires a different quantity of epoxy to be dispensed for each chip size. This problem has been overcome by the development of multi-dot machines. In operation, a small dispensing needle is used which corresponds to the smallest chip on the hybrid substrate. Several small dots are placed evenly over the die pad when larger dice are to be bonded. After all the dots have been dispensed, the collet is swung or pivoted into operation, and all the dice, which are located directly alongside the work holder, are placed on the resin. There is no need to change the collet since the resin is evenly distributed over the pad and die tilting does not occur. The position of the needle is important in controlling the size of the dot dispensed and its shape. Too low a position causes small resin dots or allows the resin to creep up the outside of the needle, which causes variations in dot size. If the needle is too high, small or point dots are produced; this results in tilting of the die.

Liquid resin dispenser systems range from the manual to fully automatic. Some types of epoxy bonders have a variable epoxy "pick and place" bonding cycle: Manual, semi-automatic or full automatic. Die bonding on this type of equipment may also be accomplished by alloying: Steady-state eutectic or pulsed eutectic. Rate of placement is 1000 to 4000 chips per hour.

In addition to paste epoxy dispensing and screening methods, the use of epoxy preforms for chip attachment has been popular in the past, but the introduction of improved paste formulations has caused a decrease in its use. At one time, the advantages of the preform were the absence of "bleed" and absence of solvents. The newer pastes, however, have improved run-out control. The introduction of high speed production equipment developed for the pastes has also limited the utilization of preforms in bonding of chips on hybrid substrates.

The technique for die bonding using preforms consists of the following operations:

(a) The preform, which is epoxy impregnated in a glass fiber mesh, is cut to the same size as the die.

(b) The preform is then placed on the bonding pad which is held at some elevated temperature to make the preform tacky.

(c) The die is positioned on the tacky preform, which serves to hold the die in place. Curing of the resin is performed by heating to the proper temperature in an oven, as with paste formulations.

3.4.3 Passive device attachment processes. The reliability of epoxy bonded chip capacitor interconnections on hybrids has been studied by Dreyer and Koudounaris.[31] In this study, chip capacitors of three different sizes and terminations were attached by conductive and non-conductive epoxy: (a) silver, palladium-silver and Sn60-Pb 36-Ag 4 alloy solder terminated devices were attached using silver conductive epoxy (Ablefilm 606-2); (b) palladium-silver terminated capacitors were bonded to the substrate using non-conductive epoxy (Scotchcast 281). Gold wires were used to electrically interconnect the Pd-Ag terminations to the substrate conductor pads.

After a sequence of environmental tests, it was found that the non-conductive epoxy was the most reliable attachment material of the two

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[31] G. A. Dreyer, A. Koudounaris and I. H. Pratt, "The Reliability of Soldered or Epoxy Bonded Chip Capacitor Interconnections on Hybrids", IEEE Trans. on Parts, Hybrids and Packaging, Vol. PHP-13, No. 3, Sept. 1977, pp. 218-224.

epoxies evaluated, and was almost equal in performance to Sn10 (10 percent Sn-88 percent Pb-2 percent Ag). It should also be noted that some hybrid manufacturers use non-conductive epoxy for attachment of the capacitor body and employ conductive epoxy under the end terminations.

3.4.4 Substrate attachment processes. Attachment of the substrate to the package base is considered to be the simplest of all bonding processes in hybrid assembly.[32] It can be performed using a paste or preform, but a preform is the generally preferred method. If a paste is applied, its deposition must be carefully controlled to provide a uniform, void-free bond. An excess of paste will tend to cause adhesive flow up and over the edges of the substrate, resulting in contamination of the substrate surface. The preform automatically produces controlled flow and adhesive film thickness uniformity. Use of a preform should eliminate the need for a visual inspection of the substrate bond area. It should also be mentioned that as larger amounts of epoxy are used under the substrate, moisture becomes more of a problem.

Brassell and Fancher[33] reported on the results of a study of four insulative epoxy adhesives for attachment of alumina substrates to metallic headers in hermetically sealed packages. Tests were conducted in this evaluation to determine the long term reliability of the epoxies and to select the most suitable adhesive for use in a high volume hybrid manufacturing facility.

The insulating adhesives chosen for evaluation were:

(a) Scotchcast 281, a one-component premixed frozen paste.

(b) Ablefilm 550, a "B"-staged epoxy impregnated fiberglass film.

(c) Epo-Tek H74 and H77, two-component systems which require mixing before use.

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[32] H. S. Kraus, "Adhesives for Microelectronics", Proceedings ISHM, 1973, Washington, D.C., pp. 3-A-5-1/3-A-5-5.

[33] G. W. Brassell and D. R. Fancher, "Electrically Insulative Adhesives for Hybrid Microelectronic Fabrication", IEEE Trans. on Components, Hybrids and Mfg. Tech., Vol. CHMT-1, No. 2, June 1978, pp. 192-197.

The test results yielded the following conclusions:

(a) Lap Shear Strength

The shear strength (aluminum to aluminum) values ranged from a high of 4000 psi (for Ablefilm 550) to a low of 1420 psi (for Epo-Tek H74) at ambient temperature.

The effects of temperature aging on lap shear strength were determined by subjecting bonded specimens (aluminum to aluminum) to 150°C for 10, 20 and 35 days prior to testing. No significant degradation of lap shear strength of any of the adhesives was observed during thermal aging; the shear strength of Scotchcast 281, Ablefilm 550 and Epo-Tek H77 all remained approximately constant over the 35-day period. The Ablefilm 550 specimens, for example, exhibited a relatively constant shear strength of approximately 4000 psi over the 35 day test period.

(b) Adhesive-Adherent Compatibility

Using the four adhesives, the lap shear strength developed between the adhesives and various adherent specimens (gold, nickel and tin-plated kovar strips) was determined.

Gold-plated kovar produced the greatest bond strengths; the values ranged from 3400 psi (Ablefilm 550) to a low of 1300 psi (Epo-Tek H74 and H77).

After thermal cycling (-55 to +125°C), the Scotchcast 281 showed no evidence of degradation after 50 and 100 cycles, but the Ablefilm 550 decreased in strength by about 25 percent after 100 cycles. It should be emphasized, however, that the final (after 100 cycles) Ablefilm 550 bond strength is much greater (about 3000 psi) than that of Scotchcast 281.

(c) Tensile Strength

Centrifuge testing was employed to evaluate the tensile strength developed between alumina substrates and gold, nickel and tin-plated kovar headers. Results show that the Scotchcast 281 yielded excellent results since no failures were obtained after stressing the test specimens at 5KG, 10 KG, 15 KG and 20 KG. The Ablefilm 550 also produced no failures, but only when a thicker (0.0075 inch) film of adhesive was used in place of the 0.003 inch thick film used originally.

(d) Thermal Properties

Degradation temperatures of the four adhesives were determined with the aid of a DuPont Model 900 TGA thermal analyzer. The quantity of outgassed products was measured for each adhesive after a 24-hour exposure at 160°C under a high vacuum of 10^{-6} torr.

The experimentally determined degradation temperatures ranged from 310°C (Scotchcast 281) to 380°C (Ablefilm 550). Cured samples, exposed to 160°C and 10^{-6} torr pressure for 24 hours, yield outgassing values (weight loss) of 3.51 percent (Scotchcast 281) to a low of 1.14 percent (Epo-Tek H77).

(e) Outgassing Effects on Electrical Devices

The effect of outgassed products on devices was evaluated by subjecting hermetically sealed hybrids to 150°C for 1000 hours and measuring the electrical parameters after 168, 500, and 1000 hours.

Each epoxy material was used to prepare three test packages: (1) thin film pattern etched from 225 ohms/square nichrome; (2) thick film pattern having 100 ohm/square and 1000 ohm/square resistor inks; and (3) thick film pattern having 10K ohm/square and 100K ohm/square resistor inks. Four transistors (2N2905A, PNP) and three diodes (1N3600) were attached to the substrate in each package using a silver conductive epoxy, which was known to have little or no effect on component behavior. Each package was solder sealed using Sn 10-Pb 88-Ag 2 solder.

Preliminary electrical test results indicated that Scotchcast 281 and Ablefilm 550 are acceptable but that Epo-Tek H77 is marginal for use in hybrid packages exposed to 150°C for long periods of time.

A recent investigation conducted by the Bendix Corporation[34] established that Ablefilm 517B and Epo-Tek H76 epoxies, in conjunction with an abraded flatpack and applied pressure during cure, were shown to provide hybrid substrate-to-flatpack bonds which met all environmental and processing requirements of hybrids produced in two recent programs.

It was determined that abrading the plated gold surface in the bottom of the flatpack (using a wet blast method) produced the best bonding surface. The wet blast method utilized 220 mesh aluminum oxide grit in a 25 to 30 percent water slurry, at 35 psi (241 kPa).

Five different epoxies were evaluated. Ablefilm 517B was selected as the epoxy for substrate attachment during production, primarily because of its use in lidding hybrid microcircuits. It was determined in the cour e of the program that an applied force during cure was required to insure complete bonding of the substrate to the flatpack. Test results indicated that a minimum pressure of 10 kPa (1.5 psi) was sufficient.

It should be noted that gaseous halogen species (ethyl chloride and/or hydrogen chloride) were detected by mass spectrometic analysis in Epo-Tek H74, Epo-Tek H61 and Epo-Tek H44. No halogen gases were detected as outgassing products of Ablefilm 517B and Epo-Tek H77.

3.4.5 Procedure for removing reject devices. Epoxy bonded reject passive and active devices are readily removed by localized heating of the chip to 125° - 150° for a few minutes.

One commercially available instrument (Model 4400 hot gas die remover, Semiconductor Equipment Corporation) uses a hot nitrogen jet to heat a small area around a reject chip without heating nearby good devices. A Z-motion capability allows the hot gas jet to be brought down into deep packages and over specific chips. A built-in die pusher is provided to break the epoxy bond, thereby eliminating cumbersome manual techniques. Brittle substrates may be preheated to prevent thermal shock.

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[34] HMC-To-Flatpack Attachment, Topical Report No. BDX-613-1800, April 1978, L.R. Zawicki, Bendix Corp., Kansas City Division.

3.4.6 Significance of results. The proper use of epoxy resins has been summarized by T aeger.[35] In the selection of materials, the epoxy resins must have a very low concentration of halogens, no sulfur and a fairly narrow molecular size distribution. The solvents must be non-chlorinated and the minimum quantity of solvent should be used. During cure, no acid type by-products should be formed. Studies performed by Licari[36] and Stanquist[37] prove conclusively that there is a definite relationship between the curing agent chemical family and its corrosion properties. The following curing agents should not be used to harden epoxy adhesives in hybrid microcircuits:

(a) primary and secondary amines

(b) polyamides

(c) boron trifluoride complexes

(d) modified heterocyclic amines

Thick film conductors are easily corroded by polyamide-cured epoxy. Gold metallization is more easily corroded than palladium-gold. These and other detailed studies[38] indicated that the tertiary amine or phthalic anhydride curing agents are more reliable for hybrid applications. In the evaluation conducted by Pietrucha and Reiss, using 200 packaged type 4001 CMOS devices, a silver-filled conductive epoxy containing phthalic

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[35] R. K. Traeger, "Organics Used in Microelectronics: A Review of Outgassing Materials and Effects," IEEE 27th Electronic Components Conference, May 16-18, 1977, (Arlington, VA), pp. 408-411.

[36] J. J. Licari, K. L. Perkins, and S. V. Caruso, "Evaluation of Electrically Insulative Adhesives for Use in Hybrid Microcircuit Fabrication," IEEE Trans. on Parts, Hybrids and Packaging, Vol. PHP-9, Dec. 1973, pp. 199-207.

[37] M. Stanquist, "Electrolytic Corrosion Attributed to Adhesives in Hybrid Assemblies", 1970 International Microelectronic Symposium (ISHM), p. 7.5.1-7.5.8.

[38] B. M. Pietrucha and E. M. Reiss, "The Reliability of Epoxy as a Die Attach in Digital and Linear Integrated Circuits", 1974 IEEE Reliability Physics Sympoisum, pp. 234-238.

anhydride catalyst was employed. Mass spectrometic analysis of the outgassed species showed the presence of H_2, O_2, Ar, CO_2, CH_4 and C_2H_6 in both the cured and uncured specimens. Water vapor was detected only in the uncured epoxy. Analysis of the outgassed species revealed no significant concentrations of ionizable compounds which might contribute to contamination-type failure mechanisms.

The best quality assurance procedure is to evaluate and qualify a given lot of epoxy material in its specific application under accelerated aging conditions.[35] Subsequent quality checks can therefore be minimal. It is suggested that the infrared spectra of new batches be compared to those of previous lots and changes in spectral results should be looked for. Thermogravimetric analysis of the cured resin will show the presence of unexpected volatiles resulting from incorrect formulation and/or inadequate cure.

Application of epoxy resins for initial device attachment or rework should be carried out using procedures considered to be good practice for handling and fabricating microcircuits, which includes:

(a) curing in a circulating air oven with constant air purge,

(b) maintenance of clean and dry processing conditions,

(c) curing at least at the maximum time and temperature which will be seen in subsequent processing or use,

(d) to minimize moisture contamination, hybrids must be subjected to vacuum bake prior to sealing. The bake temperature and time required must be determined during process qualification.

(e) hybrids containing epoxy adhesives must be stored in a dry atmosphere to prevent moisture absorption,

(f) hybrids containing epoxy must not be exposed to strong organic cleaning solvents such as trichlorethylene and trichloroethane,

(g) epoxy bonded hybrids must not be heated over the cure temperature of the epoxy materials used.

(h) A low "bleed out" resin should be used, not only to insure clean bonding pads (on the substrate) for the initial wires but to provide an epoxy-free bonding surface for subsequent wire bonds during rework.

(i) A very reliable non-metallurgical method of attachment of chip capacitors to substrates is bonding using non-conductive epoxy, with 0.002 inch diameter gold wire interconnects. At higher frequencies of microcircuit operation, the resistance of the wire is detrimental to circuit performance. The use of conductive epoxy is not recommended, however, in view of the very high mechanical failure rate experienced in the Hughes study.[14] To eliminate the resistance of the wires for high frequency applications, and to minimize the incidence of electrical and mechanical failures, it is recommended that an appropriate high melting point solder, such as Sn 10 solder alloy (10 Sn/88 Pb/2 Ag, M.P. = 299°C) be considered as the ceramic chip capacitor attachment material, using (a) palladium-silver end terminations, (b) large bonding pads (0.140 x 0.105 inch) and reflow soldering of Sn 10 tinned substrate pads. An alternate procedure is to use both conductive and non-conductive epoxy as discussed in section 3.4.3.

(j) Silicon device chips bonded to thick or thin film substrates, using either conductive or nonconductive epoxy, produce a very reliable bond that withstands device push-off tests and MIL-STD-883 environmental tests:

(1) mechanical shock, method 2002.2, condition C (3000G, 20 pulses, Y1 direction).

(2) constant acceleration, method 2001.2, condition B (10,000G, Y1 direction).

(k) visual examination is of minimal value in detecting marginal ceramic (K1200) capacitor chip attachments.

(l) constant acceleration or mechanical shock (preceded by thermal cycling) are the most effective environmental screening procedures for detecting electrical failures in conductive epoxy bonded chip capacitors.

3.5 Task IV - Interconnect rework.

3.5.1 General. At the present time, there are four predominant chip interconnection techniques used in the assembly of hybrid microcircuits. Three of these are considered to be face bonding systems and the fourth, beam lead bonding, is classified as a modified terminal system:[39]

(a) Thermocompression and thermosonic ball bonding.

(b) Wedge ultrasonic bonding.

(c) Beam lead bonding.

(d) Flip chip bonding.

Although other types of interconnection bonding are used in hybrids (such as gold ribbon "welding" to connect the substrate to the package leads), the aforementioned four types are most commonly used in hybrid assembly and are subject to the controls of MIL-M-38510 and MIL-STD-883. Newer techniques, such as the tape carrier process, are still under development for hybrid applications and therefore will not be considered as a mature interconnection process.

In the hybrid industry today, there is a need for two types of wire bonders: one for the low volume, high complexity, more expensive circuits required for military and space applications and one for the high volume, low density, lower cost hybrids that are needed for the consumer market. Manual bonders are currently being used for most hybrid assembly but the high volume consumer market is forcing a conversion to automated wire bonding.

It should be noted that beam lead and flip chip bonding are not only a method of interconnection but also one of chip attachment to the substrate.

3.5.2 Device interconnect techniques.

1. Thermocompression Ball Bonding. For many years, this method was very popular as an interconnection process for active device chips on

[39] H. E. Thomas, Handbook of Integrated Circuits, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1971, pp. 169-191.

complex hybrid substrates, but is now being replaced by aluminum ultrasonic or gold thermosonic bonding. Ball bonding uses gold wire only. A ball of gold is typically formed by means of a hydrogen flame, then squeezed by a capillary to form a large area of thermal compression bonding. The second bond is a wedge bond, usually made on the substrate bonding pad.

(a) In conventional thermal compression ball bonding, the temperature of the gold-chip bonding pad interface is heated to 150°-200°C. Most of the heat is furnished by the substrate heater to produce interface temperatures of 150°C to 200°C.[40][41]

(b) Pulsed thermocompression (PTC) bonding, on the other hand, typically uses an interface temperature of 300°C to 350°C, for dwell periods up to a few seconds duration.[40] The capillary is also heated during the bonding operation.

(c) During thermosonic (ultrasonic gold ball) bonding, ultrasonic energy is transmitted to the capillary during the thermocompression operation. The substrates are heated, usually to 100-150°C, prior to initiation of the bonding operation. A major advantage of the thermosonic process is the lower substrate temperature required during bonding.

2. Wedge Ultrasonic Bonding. This technique is generally limited to the formation of wedge/wedge bonds of aluminum wires to chip bonding pad and substrate metallization. A wedge-shaped tool is used, which flattens the wire and forms a cold welded joint beneath the flattened region. The typical hybrid ultrasonic bond is made by ultrasonically scrubbing a 0.001 inch diameter aluminum wire back and forth, under moderate pressure and without applied heat, across the bonding pad of an active device or

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[40] J. L. Jellison, IEEE Trans. on Parts, Hybrids and Packaging, Vol, PHP-11, p. 206-211, 1975.

[41] T. H. Ramsey, Solid State Technology, p. 43, October 1973.

the gold coated surface of the substrate bonding pad. The scrubbing process removes oxides and other contaminating films from the surface that may prevent formation of a cold welded interface.

The metallurgical bond is achieved by plastic deformation of the wire under a force of 0.25-0.49 newtons with simultaneous ultrasonic vibration at 40-60 Hz.[42]

3.5.3 Significance of results.

1. Thermocompression/Thermosonic Ball Bonding and Wedge Ultrasonic Bonding. Rebonding to the gold or aluminum bonding pad of a device must be performed under certain conditions, to insure bond reliability:

(a) No more than one rebond attempt should be attempted on a given bonding pad location on the chip.

(b) At least 50 percent undisturbed chip metallization should be under the bond.

(c) A rebond should not touch an exposed region of oxide (silicon dioxide) caused by lifted metal.

Surface contamination can seriously affect the integrity of a thermocompression ball bond. The chip and substrate metallization systems may be contaminated by various types of soils, both organic and inorganic. Most hybrid microcircuit assemblies, if contaminated prior to or during rework by trace quantities of these soils, may be cleaned by vapor degreasing in Freon TF.

Excessive contamination on the designed bonding areas, such as uncured or cured epoxy, would be more difficult to remove.

The major contaminants that may affect rebondability of gold and aluminum wires to thick/thin film substrate metallization are:

(a) Epoxy films on substrate conductor runs and on semiconductor chip bonding pads.

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[42] D. W. Bushmire, Solid Phase Bonding, SAND75-0177, Sandia Laboratories, June 1975.

(b) Copper oxide films on thin film gold.

(c) Chromium oxide films on thin film gold.[43]

(d) Photoresist residue on thin film gold conductors.[43]

(e) Body oils on substrate conductor runs.

It is necessary to determine the compatibility of <u>each</u> circuit component material with the proposed cleaning solvents prior to cleaning the assembled hybrid. Even the less active solvents, such as Freon TF, are known to attack and dissolve the organic insulation coatings from magnetic components, such as toroid inductors.

Although the Freon TF cleaning method is effective for moderate levels of solvent-soluble organic contamination, the presence of excessive amounts of organic contaminants, such as cured epoxy or photoresist residue over a substrate bonding pad, requires the implementation of more drastic cleaning procedures.

Bonham and Plunkett[44] have investigated the application of oxygen plasma to clean hybrids just prior to wire bonding. The technique involves the utilization of RF power to generate oxygen free radicals, which then react with organic hydrocarbons to produce water vapor, carbon monoxide and carbon dioxide, which are then pumped from the cleaning chamber. Hybrid microcircuits use many materials that are readily oxidizable, such as: nichrome and tantalum nitride resistors, silver metallization and epoxy adhesives. Consequently, the concentration of oxygen radicals and the time of hybrid exposure must be carefully controlled to prevent changes in the electrical characteristics of active and passive devices.

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[43] <u>Evaluation of Pre-Bond Etchants in Hybrid Microcircuit Processing</u>, SLA-73-1049, P.H. Holloway and R. L. Long, Sandia Laboratories, November, 1973.

[44] H. B. Bonham and P.V. Plunkett, "Plasma Cleaning for Improved Wire Bonding on Thin Film Hybrids," <u>Electronic Packaging and Production</u>, February, 1979, pp. 42-55.

The advantages of the application of plasma cleaning to the wire bond rework process are obvious; the plasma cleaning step may be utilized after solvent cleaning to remove organic films (such as epoxy "bleed-out" films) not dissolved by the solvent cleaning process. In some instances, a trace of organic contamination may be deposited after solvent cleaning as the consequence of a slight solubility of one of the organic materials (such as epoxy) in one of the solvents employed. A carefully controlled final cleaning by oxygen plasma would eliminate the contaminating film and insure formation of a reliable metallurgical bond.

The plasma cleaning process is currently in use or under evaluation by various manufacturers of military grade hybrids, including Hughes Aircraft Company, Teledyne Microelectronics and General Dynamics. As with all cleaning processes, the plasma cleaning method must be qualified for each type of active or passive device employed in fabrication of the hybrid.

B. Package Cleaning Procedures. In addition to organic contaminants, numerous metallic impurities such as copper, chromium, silicon, cobalt, nickel, iron, titanium, and silver have been associated with poor bonding characteristics of gold wires to package surfaces. The degradation of TC gold ball bond strengths due to the presence of metallic films has long been suspected.[45][46] Gold is typically plated over a kovar or nickel substrate (of a package) for adhesion. The presence of discoloration after a package bake cycle is attributed to the diffusion of the substrate material (Fe, Ni, Co) through the gold to the surface, where it oxidizes. These metallic residues can be removed and bondability to the package element can be restored by chemically etching the contaminating film with either a gold etch treatment (using $KI + I_2$) or a metal oxide etch (using ceric ammonium nitrate). Organic residues may be removed from package surfaces by

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[45] G. E. McGuire, J. V. Jones and H. J. Dowell, "The Auger Analysis of Contaminants that Influence the Thermocompression Bonding of Gold," Thin Solid Films, Vol. 45, 1977, pp. 59-68

[46] C. W. Horsting, "Purple Plague and Gold Purity," Proc. IEEE Reliability Physics, April 5-7, 1972, pp. 155-158.

oxygen plasma etching or by exposure to ultraviolet light and reaction with ozone.[47]

C. Evaluation of Wire Bonding Process Variables. An intensive study of the effects of wire bonding processing variables, substrate metallizations and in-process tests was conducted by Hughes.[14] The evaluation was performed using:

(a) thin film gold (Au over Ni over nichrome) and thick film (fritted or fritless) gold metallization. The fritless gold had a copper additive.

(b) pulsed thermocompression gold wire bonds: 1 mil and 2 mil diameter gold wire.

(c) ultrasonic aluminum (wedge) bonds: 1 mil diameter aluminum (1 percent silicon)

The significant findings of this study[14] were:

1. Ultrasonic Aluminum Wire Bonds (0.001 inch diameter, 1 percent Si). Changes in the force, power and time settings of the bonding have a strong influence on bond strength. Force and power variations had a slightly greater influence than variations in time. Failure to establish optimum bonding parameters can also result in "cratering" of bonding pads, in which the silicon or SiO_2 layer under the aluminum is cracked, ultimately resulting in device electrical failure.[48]

Nondestructive bond pull testing at 1 gram force was either slightly beneficial or had no effect on bond strength. The 1 gram test usually increased the average bond strength when the aluminum wires were subjected to a destructive pull test. Nondestructive testing at 2 grams force either slightly increased or slightly decreased the mean bond strength. During

[47] J.R. Vig and J.W. LeBus, "UV/Ozone Cleaning of Surfaces," IEEE Trans. Parts, Hybrids and Packaging, Vol. PHP-12, December, 1976, pp. 365-370.

[48] V.S. Kale, "Control of Semiconductor Failures Caused By Cratering of Bonding Pads," Proceedings ISHM, 1979, pp. 311-318, Los Angeles, CA.

destructive testing of as-bonded wires, the failure mode was fracture in the necked-down region of the wire next to the bond pad. Only bonds to thin film and thick film fritless gold were influenced by nondestructive testing at 1 gram and 2 grams force; bonds to thick film fritted gold were not influenced by nondestructive pull tests at 1 or 2 grams.

Exposure of the wires at 150°C (for 168 hours) did not affect the strength of bonds to thin film or fritless gold metallization. The 150°C high temperature storage annealed the aluminum wires, which lowered the bond strength from about 10 grams to 5 grams. The failure mode after the 150°C exposure was the same as before the thermal aging; failure occurred by fracture of the wire in the necked down region of the wire.

Ultrasonic aluminum wire bonds to the fritted thick film gold experienced a large decrease in pull strength after the 150°C thermal aging step. The as-prepared bond strengths were 9-12 grams but after the 150° exposure, these values decreased to approximately 3 grams average. Bond failures were characterized by lifting or tearing of the bonds from the fritted gold metallization layer. These observations are consistent with the results of other studies of aluminum wire bonding to thick film gold conductors.(49)(50)

It was not possible to separate the effects of bonding machine or operator dependence. Both factors apparently can alter resultant bond behavior, with operator dependence probably having the greater effect.

There was no noticeable difference between substrate-to-substrate and chip-to-substrate bond behavior. Although a consideration of geometry would suggest some variances, the loop heights of both types of bonds were approximately the same; it was concluded, therefore, that the addition of the 5 mil chip height at one end of a wire loop was apparently not significant.

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(49) J.D. Prather, S.D. Robertson and J.W. Slemmons, "Gold Thick Film Conductors for Aluminum Wire Bonding," 1974 International Microelectronics Conference West, pp. 34-42.

(50) W.R. Rodrigues de Miranda and R.G. Oswald, Proceedings ISHM, 1974, pp. 228-244.

Substrate type and metallization produced some variations in bond strength, but, except for bonds made to the fritted gold, the differences were minor. Comparison of average bond strengths (after the 150°C, 168 hour exposure) showed that thin film gold (on glazed alumina) and thick film fritless produced the strongest bonds whereas the bonds on thick film fritted gold were about one-half as strong.

2. Pulsed Thermocompression Gold Wire Bonds (0.001 inch diameter). Bonding schedule temperature settings strongly affected the strength of gold wire bonds to thin film gold on glazed alumina substrates.[14] Bonding to thin or thick film metallization on unglazed alumina indicated there was only a moderate effect on gold-to-gold bond strength due to schedule variations of force, temperature or time at temperature.

Destructive pull testing showed that bond strengths were not affected by previous stressing of the wires during a 1 gram or 3 gram nondestructive test.

Gold wire bonds to thick film gold metallized substrates, especially the fritless gold, became stronger after high temperature exposure (150°C, 168 hours). Bonds to thin film gold were not affected, but the gold bond to the chip severely weakened. Most of these bonds failed at very low strengths with the bonds lifting from the chip (aluminum) surface. It was believed that the temperature at the chip — gold ball interface was too high during bonding, which initiated the formation of one or more intermetallic phases, which then grew further during storage at 150°C. The high bonding temperatures experienced in this evaluation would not have been necessary if a heated stage had been used. Under conventional hybrid manufacturing conditions using gold wire-to-chip bonding, a heated stage is always used and bond failures of this type are not normally encountered.

According to a thermosonic wire bond study conducted by Johnson and Chavez,[51] their objective was to assess not only the quality and performance

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[51] D.R. Johnson and E.L. Chavez, "Characterization of the Thermosonic Wire Bonding Technique," Proceedings ISHM, 1976, 11. 88-95.

of the gold wire bonds when exposed to thermal environmental tests, but also to ascertain the process control parameters required to reproducibly fabricate reliable bonds. It was concluded from this study that the thermosonic technique eliminates the need for special pre-bond etching and cleaning procedures used in production of Sandia hybrid microcircuits. It was also found that the thermosonic process allowed a wider variation in bonding parameters, which, when coupled with the lower required substrate temperature of about 100°C, presents many advantages compared to the relatively rigid process controls required for thermo-compression bonding.

3.6 Task V - Package replacement.

3.6.1 General. Although most hybrid rework is accomplished before package sealing, component failure during burn-in or other acceptance tests would normally require at least one delidding step. If the lid seal cannot be repaired, it becomes necessary to remove the substrate (and mounted components) and place it in a new package. Other common causes of package replacement are cracked glass bead-metal lead seals and broken leads. Epoxy bonded substrates only should be removed.

Much of the activity involved in this task is also discussed in Tasks I, II, III and IV. In particular, Section 3.4.4 of Task III and Section 3.3.6 of Task II consider the use and limitations of polymer and metallurgical methods, respectively, for the attachment of substrates to package bases.

Techniques for removing substrates may be classified as follows:

(a) Mechanical

(b) Chemical

(c) Thermal

The design of the hybrid should be compatible with a possible package replacement rework requirement. The layout of the substrate and interconnect wires should be made with rework in mind; the substrate bonding pads could be made larger to accommodate a second wire bond connecting the substrate to the package.

3.6.2 Methods of substrate removal.

1. Mechanical Methods. Generally, a mechanical force is carefully applied to detach the substrate from the package base. When combined with thermal or chemical techniques, the length of time (of force application) or the temperature required, can be decreased.

After the substrate is removed from its base, the interconnections must be repaired. There are two approaches often utilized to facilitate rework of the package-to-substrate interconnections: (a) fabricating sufficiently large substrate pads to provide new bonding sites or (b) using sufficiently long wires to permit rebonding.

2. Chemical Methods. Most epoxies used in hybrid microcircuits are softened or dissolved by solvents. As a consequence, substrate detachment can be achieved in principle using the proper solvent or combination of solvents. Extreme care must be exercised to prevent (a) attack of the epoxies used for a device attachment, resulting in a weakened device-to-substrate bond, (b) chemical degradation of aluminum wires and aluminum bonding pads on silicon devices, or (c) contamination of the various circuit elements with epoxy films due to chemical attack and dissolution of the various epoxy bonds by organic solvents.

3. Thermal Methods. Thermal techniques are, in general, the best suited procedures for removing substrates attached to package bases by alloys and non-conductive epoxies.

For alloy bonded substrates, attention must be given to the temperatures required. In practice, the sequence used in mounting alloy bonded devices and alloy bonded substrates determines the melting points of the alloys to be selected and the difficulties encountered in rework of devices and package replacement.

3.6.3 Significance of Results. The significant findings of package replacement studies were discussed in Sections 3.3.6, 3.3.7, 3.4.4 and 3.4.6.

4.0 SURVEY OF INDUSTRY PRACTICE ON HYBRID MICROCIRCUIT REWORK

4.1 Definition of hybrid rework. Since the objective of the program is the modification of existing MIL-M-38510 rework requirements and the establishment of rework guidelines, it is advisable to define the concept of rework at the outset.

For convenience, a typical face-up chip and wire hybrid microcircuit manufacturing process sequence (shown in Figure 4) has been employed as the vehicle to develop a suitable definition of hybrid microcircuit rework. The need for in-process repairs may be indicated at various points in the assembly, screening or testing processes utilized in the production of the hybrid.

Examination of the various processing steps suggests that hybrid rework can be categorized into six different source types. The six sources are listed in the order in which they occur in the hybrid manufacturing process:

(a) Operator requested rework during fabrication or assembly, in which the hybrid is returned to a previous process operation for repair. Documentation of rework commences at this point.

(b) Line inspection (by an operator) of the completely assembled hybrid. This is an optional requirement.

(c) First (pre-seal) electrical test, usually a functional type test.

(d) Q.A. pre-seal visual inspection.

(e) Sealing operation and post sealing acceptance tests, which include: leak tests, PIND test and other electrical, mechanical and environmental tests. The acceptance tests also detect damage resulting from the sealing process itself.

(f) Q. A. final inspection

Each of the rework procedures must be qualified before application on the manufacturing line. Assembly personnel must be certified for their assigned rework operations to assure proficiency in their rework process areas.

In addition to the aforementioned six sources of documented rework, there is an area of the process flow in which undocumented fault correction is frequently performed. At the beginning of the hybrid fabrication and assembly process sequence, a fault may be corrected by the operator who was responsible for creating the defect. As an example, the resistor trim operator makes a final check of the resistor values on a substrate and finds that one resistor is marginal or still outside specification, which requires additional trimming. This corrective step is not considered to be rework. This fault correction activity generally occurs prior to permanently bonding the substrate to the package.

Table 8 presents a breakdown of typical specific defects corrected by each of the six typical sources of rework.

Based on an analysis of the various sources of rework, a definition of rework has been formulated:

Rework is the repeating of a previous manufacturing process step and is performed to replace (or improve the condition of) a defective or out of specification hybrid microcircuit element. It consists of the correction or removal (and replacement) of defective hybrid components as determined by in-process screening tests, visual inspection and electrical tests. These corrective procedures may be employed before or after package sealing to eliminate the condition of nonconformance with the specification, drawing or other approved product description.

Rework occurs, therefore, when an inspection or test step indicates that (1) a previous process operation has resulted in a condition that is outside the limits of the process or test specification, (2) a defective component has been used in assembly. Under these conditions, the hybrid must be returned to one or more previous process operations for documented correction of the fault(s). Repair, on the other hand, is a corrective action that reduces but does not eliminate the condition of non-conformance.

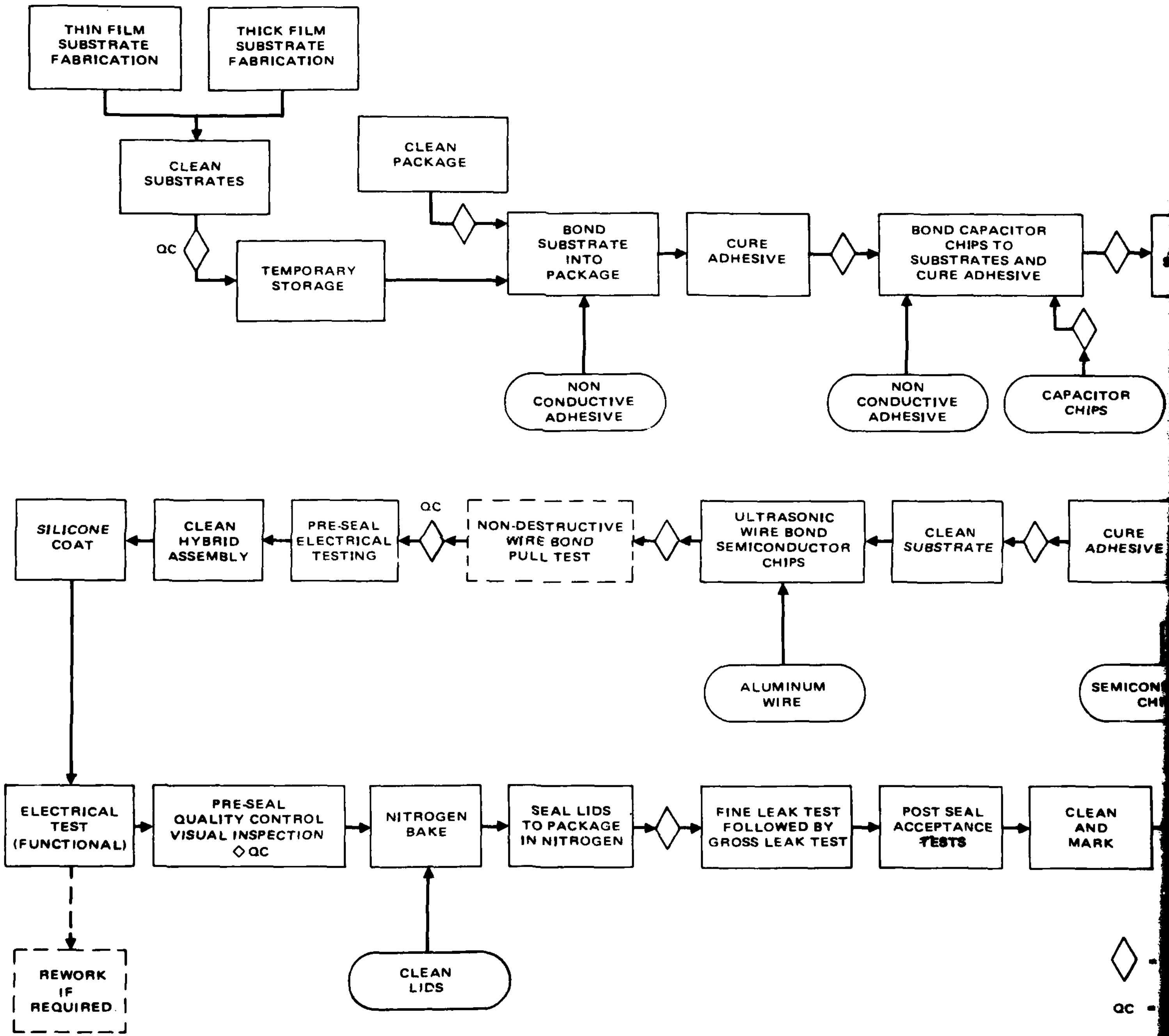
THIN FILM SUBSTRATE FABRICATION
THICK FILM SUBSTRATE FABRICATION
CLEAN SUBSTRATES
CLEAN PACKAGE
QC
TEMPORARY STORAGE
BOND SUBSTRATE INTO PACKAGE
CURE ADHESIVE
BOND CAPACITOR CHIPS TO SUBSTRATES AND CURE ADHESIVE
NON CONDUCTIVE ADHESIVE
NON CONDUCTIVE ADHESIVE
CAPACITOR CHIPS
SILICONE COAT
CLEAN HYBRID ASSEMBLY
PRE-SEAL ELECTRICAL TESTING
QC
NON-DESTRUCTIVE WIRE BOND PULL TEST
ULTRASONIC WIRE BOND SEMICONDUCTOR CHIPS
CLEAN SUBSTRATE
CURE ADHESIVE
ALUMINUM WIRE
SEMICON
CHI
ELECTRICAL TEST (FUNCTIONAL)
PRE-SEAL QUALITY CONTROL VISUAL INSPECTION ◇ QC
NITROGEN BAKE
SEAL LIDS TO PACKAGE IN NITROGEN
FINE LEAK TEST FOLLOWED BY GROSS LEAK TEST
POST SEAL ACCEPTANCE TESTS
CLEAN AND MARK
REWORK IF REQUIRED
CLEAN LIDS
QC -

Figure 4. P

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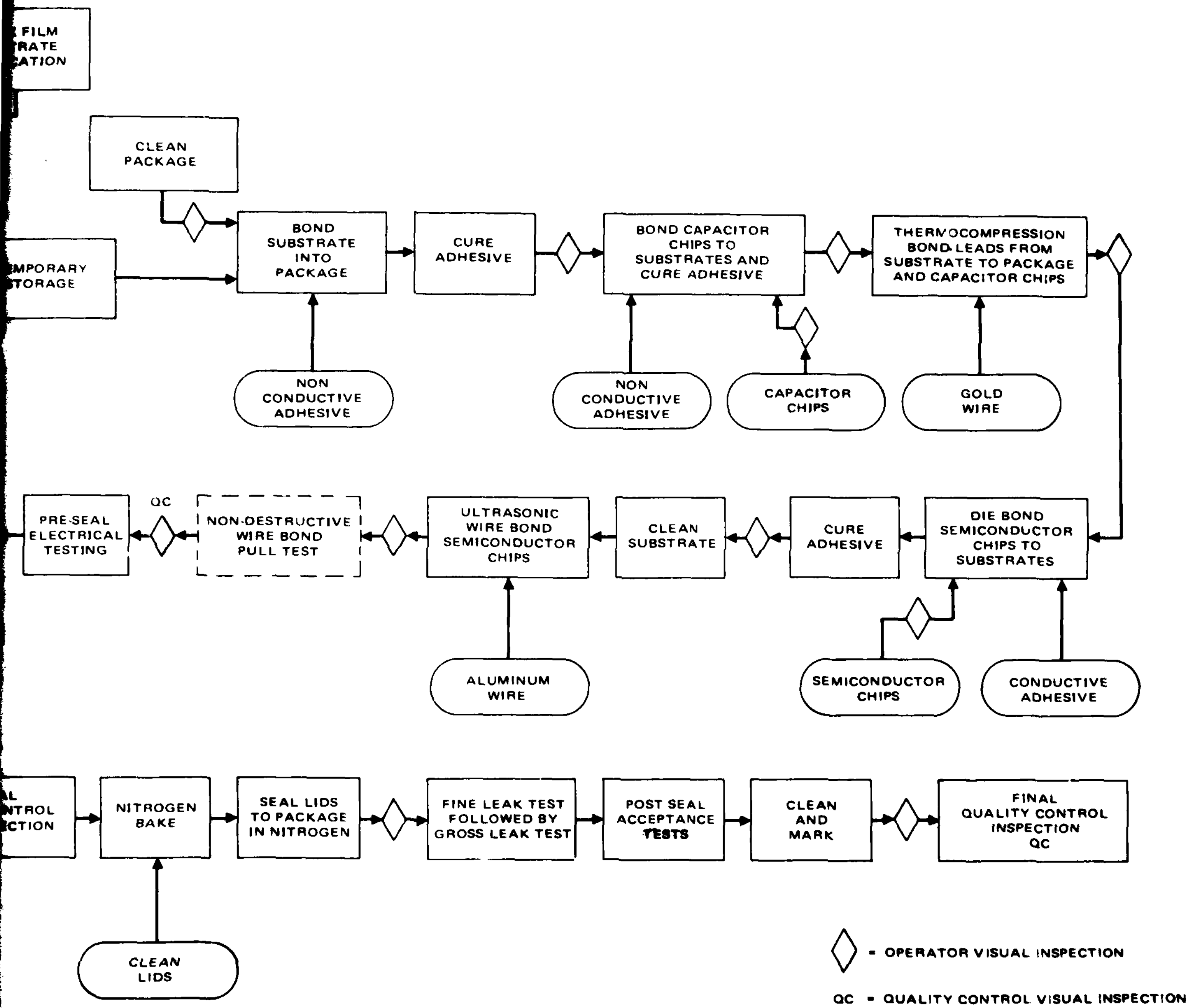

Figure 4. Process flow for typical face-up chip and wire hybrid microcircuit.

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TABLE 8. TYPICAL SOURCES OF HYBRID MICROCIRCUIT REWORK

Operator Requested rework (during assembly)	Line inspection	First electrical test	Q.A. pre-seal Visual inspection	Sealing operation and post-seal acceptance tests	Q.A. final inspection
Replace substrate	Wire dressing	Replace devices	Wire dressing	Solder and weld splatter	Package damage
Replace devices	Wire replacement	Replace wires	Wire placement	Deformed and broken wires	Lead damage
Replace wires	Missing wires	Add wires	Missing wires	Component damage	Improper marking
Damage in handling	Contamination	Trim resistors	Contamination	Leakers	Cosmetic scratches
	Component and substrate damage		Misorientation (of components)	Defective devices	Contamination
	Component and substrate orientation		Component damage		Solder splatter
	Package damage		Substrate damage		
			Fillets		
			Wire Height		
			Wire length		
			Wires crossing		
			Package damage		
			Substrate conductor damage		

4.2 Survey of hybrid microcircuit manufacturers. A telephone survey of military grade hybrid manufacturers was conducted to acquire the following information:

(a) Which manufacturing processes are most widely used?

(b) How closely is MIL-M-38510 adhered to?

(c) The nature and extent of rework of hybrid microcircuits.

(d) Which controls are utilized to maintain quality assurance for reworked hybrids?

(e) Any comments regarding MIL-M-38510.

Twenty one hybrid manufacturing facilities were contacted. Their annual production rates of military type hybrids ranged from a few thousand to over one hundred thousand. The results of the survey are summarized in Table 9.

The large manufacturing facilites had a variety of different programs whose requirements were controlled by their customers; therefore, hybrids with different assembly techniques were produced in the same facility.

The majority of the hybrid facilities surveyed use metallic packages with a seam welding sealing process. Epoxy is widely used for substrate and device attachment. Considerable differences exist, however, in methods employed for interconnecting chip capacitors. The majority of the manufacturers surveyed use conductive epoxy, but the gold wire pulsed thermocompression bonding process for chip capacitor interconnection is gaining in popularity.

There are also major differences in the wire bonding processes employed. Surprisingly, the most popular method for interconnecting active device chips to the substrate is the thermosonic gold ball bonding process. The major reasons for its popularity are its low processing temperature, tolerance to wide variations in process variables, capability of automation and the non-degrading characteristics of gold wire bond strength at elevated temperatures. In the course of the survey, no manufacturer expressed any difficulties due to the formation of gold-aluminum intermetallics. The

Manufacturer Code	Annual Volume, 1000's of Hybrids	Package Type		Package Seal			Substrate		Subst. Attach		Chip Attach		Chip Capacitor Attach			Wire Bonding					Follow MIL-M-38510(1) Without Exceptions	Follow MIL-M-38510(1) With Exceptions	Types of R Allowed by		
		Metallic	Ceramic	Solder	Braze	Weld	Thin Film	Thick Film	Epoxy	Eutectic	Epoxy	Eutectic	Cond. Epoxy	Solder/Braze	Au Wire Bond	Al - US	Au - TC	Au - PTC	Au - TRS	Au - Weld			Wire Bond Replacement	Chip Replacement	Capacitor Replacement
A	>100		X	X		X	X	X	X	M	X	M			X		X		M	X	Yes	Yes	X	X	X
B		X	X	X	X	X	X	X	X	M	X	M	X			X			X		Yes	Yes	X	X	X
C		X				X	M	X		X		X		X			M		X		Yes	Yes	X	X	X
D		X	X	X	X	X	X	X	X	M	X	M			X			M	X		Yes	Yes	X	X	X
E		X	X		X	X	X	X	X	M	X	X		X		M			X		No	Yes	X	X	X
F		X	X	X	X	X	X	X	X	X	X	X	X			M			X		Yes	Yes	X	X	X
G		X	X	X	X	X	X	X	X	X	X	X	X			X			X		Yes	Yes	X	X	X
H		X			X	M	X	X	X	M	X	M	X	M		X	M		X		No	Yes	X	X	X
I		X	X	X	X	X	X	X	X	X	X	X	X	X		X	X		X		Yes	Yes	X	X	X
J	10 - 100	X	X	X		X	X	X	X	X	X	X	X						X		No	Yes	X	X	X
K		X			X	X		X	X		X		X			X		X			No	Yes	X	X	X
L		X	X	X	X	X	X	X	X	M	X	M	X		X		X		X		No	Yes	X	X	X
M		X	X		X	X	M	X	X		X	M	X						X		No	Yes	X	X	X
N		X		X			X	X	X	X	X	X		X			X		X		No	Yes	X	X	X
O		X	X	X		X	X	X	X		X				X	X		X	X		No	Yes	X	X	X
P	<10	X	X	X	X	X	X	X	X		X				X				X		No	Yes	X	X	X
Q		X				X	X	X	X		X		X			X			X		No	Yes	X	X	X
R		X				X	X	X	X	M	X			X	X	M		X	X		No	Yes	X	X	X
S		X	X	X	X		X	X	X	M	X	M	X	X		X		X			No	Yes	X	X	X
T		X			X	X		X	X		X		X			X	X	X	X		No	Yes	X	X	X
U		X	X		X	X		X	X		X		X					X	X		Yes	Yes	X	X	X

O = Not Permitted
M = Minimum
U = Undefined
MRB = As determined by a Material Review Board
NDP = 100% Non-Destructive Pull Test
(1) = MIL-M-38510 is followed only when imposed by the customer
US = Ultrasonic
PTC = pulsed thermo compression
PC = thermocompression
TRS = thermosonic

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TABLE 9. SUMMARY OF REWORK PERFORMED BY THE MILITARY GRADE HYBRID MICROCIRCUIT INDUSTRY

MIL-M-38510(1) With Exceptions	Types of Rework When Allowed by Customer: Wire Bond Replacement	Chip Replacement	Capacitor Replacement	Substrate Replacement	Package Replacement	Rework After Seal	Number of Reworks Allowed: Before Seal	After Seal	Controls for Rework: 100% N.D.P on Rework	Rework Documented	QA Visual Acceptance	Env. and El Acceptance	M.R.B.	Comments by the Manufacturer
Yes	X	X	X	X	X	X	U	U		X	X	X		Properly executed rework does not degrade quality of hybrid.
Yes	X	X	X	X	X	X	U	U		X	X	X		Properly controlled rework does not degrade the reliability of hybrid
Yes	X	X	X			O	U	O			X	X		After seal, hybrids are scrapped if they fail env. or el. accept. test
Yes	X	X	X			X	2	1		X	X	X		
Yes	X	X	X	X	X	X	U	2		X	X	X		Eutectic rework should be done with conductive epoxy
Yes	X	X	X	X	X	X	U	MRB	X		X	X	X	Eutectic rework should be done with conductive epoxy
Yes	X	X	X	X	X	X	U	U		X	X	X		Most people do not understand MIL-M-38510.
Yes	X	X	X			X	3 total			X	X	X		PIND failures should allow rework by piercing package.
Yes	X	X	X			O	3	O	X	X	X	X		Rework should be controlled by economic feasibility.
Yes	X	X	X	X	X	X	U	1		X	X	X		Rework process instructions and training must be established.
Yes	X	X	X			O	3	O			X	X		
Yes	X	X	X	X	X	X	3 total		X	X	X	X		All rework must be documented on travelers.
Yes	X	X	X	X	X	X	6	MRB		X	X	X	X	MIL Spec should be revised to reflect rework being performed in the industry.
Yes	X	X	X	X		MRB	MRB	MRB		X	X	X	X	MRB should control nature and extent of rework
Yes	X	X	X	X	X	X	U	U		X	X	X		

aluminum wire bonding process is still used in the military hybrid industry and many facilities maintain this capability to satisfy customer requirements.

All the companies surveyed are directly or indirectly producing hybrid microcircuits according to MIL-M-38510 requirements. Only a small minority of military hybrids are produced without exceptions to MIL-M-38510. The reasons for this are purely economical. The complexity of hybrid microcircuits is such that it is difficult to have a high production yield without rework. The most critical factor is the performance of the monolithic integrated circuits devices. Hybrid manufacturers are responsible for the electrical performance of their delivered hybrids. The complexity and the performance of the integrated circuits determine the yield, which in turn governs the profit. MIL-M-38510, by restricting rework, increases the hybrid manufacturing cost.

For this reason, the majority of hybrid manufacturers prefer to develop their own specifications, based on MIL-STD-883 and MIL-M-38510, but allowing a wider range of rework.

There were major differences in rework philosophy between the various hybrid manufacturers. Usually, those manufacturers that have initiated personnel training programs and have developed special rework instructions, acceptance criteria, and documentation do not fear rework. Their reworked hybrids are just as good as non-reworked hybrids. The greatest objections to rework come from those facilities that had experienced poor rework results due to the use of improper processes and the lack of rework process controls.

The extent of rework is summarized in Table 9. Wire, chip and device replacements were common and often were treated as a normal part of the hybrid assembly. Substrate and package replacement rework were also a common practice. Of the twenty-one facilities contacted, only four did not allow rework after package seal as their standard practice. Other facilities who build hybrids to MIL-M-38510 do not rework hybrids after seal only as a contractual requirement. All the manufacturing facilities contacted require reworked hybrids to pass visual, electrical and environmental acceptance criteria. The majority of these facilities require documentation of rework. Some require 100 percent nondestructive wire bond pull tests on reworked chips and Material Review Board (M.R.B.) disposition.

5.0 EXPERIMENTAL PROCEDURES

The overall experimental approach used in this program is described in Section 1.3. Details of the technical procedure are presented in the following section.

5.1 Test hybrid design. A standardized hybrid test specimen was designed and fabricated to test all the parameters covered by Tasks I through V. The packages used were a) 1 x 2 inch ceramic axial lead packages with solderable lids and b) 1 x 2.3 inch Kovar packages with glass-to-metal seals, a weldable lid and a brazeable lid.

The test substrate used in this program is shown in Figure 5. Thick film substrates were fabricated with ESL 8880 fritless gold conductors, ESL 3800 100 ohms/square resistors and ESL 4771B resistor overglaze. Substrates used for eutectic device and substrate attachments were also metallized with ESL 5800B platinum/gold on the chip bonding pads and on the back side of substrate. Thin film substrates were prepared from slides suitable for soldering, with a thick nickel barrier on both sides of the substrate. Resistors were not trimmed.

Each test hybrid package contained three identical substrates. Substrate number 1 is the control substrate; no repair was done on this substrate. The objective was to determine whether any rework performed on substrates number 2 and 3 influenced the performance of substrate number 1.

The experimental approach was based on the detection of wire bond degradation and failures during environmental testing. This technique permits determination of the (a) quantity of lifted wire bonds, (b) change by the wire bond electrical resistance by measuring the increase in resistance along a row of shorted (series) resistors and (c) the change in wire bond pull strength. Series resistors are shorted by wire bonds either from substrate pad to substrate pad or from device pad to substrate pad. The series resistors on each substrate are shorted by a) sixteen aluminum and sixteen gold wires to bond eight transistor chips to substrate pads, b) ten aluminum and ten gold wires to form substrate pad interconnections, c) twenty-four gold wires to bond substrate pad to six chip capacitors. Figures 6 and 7 are typical as-assembled hybrids.

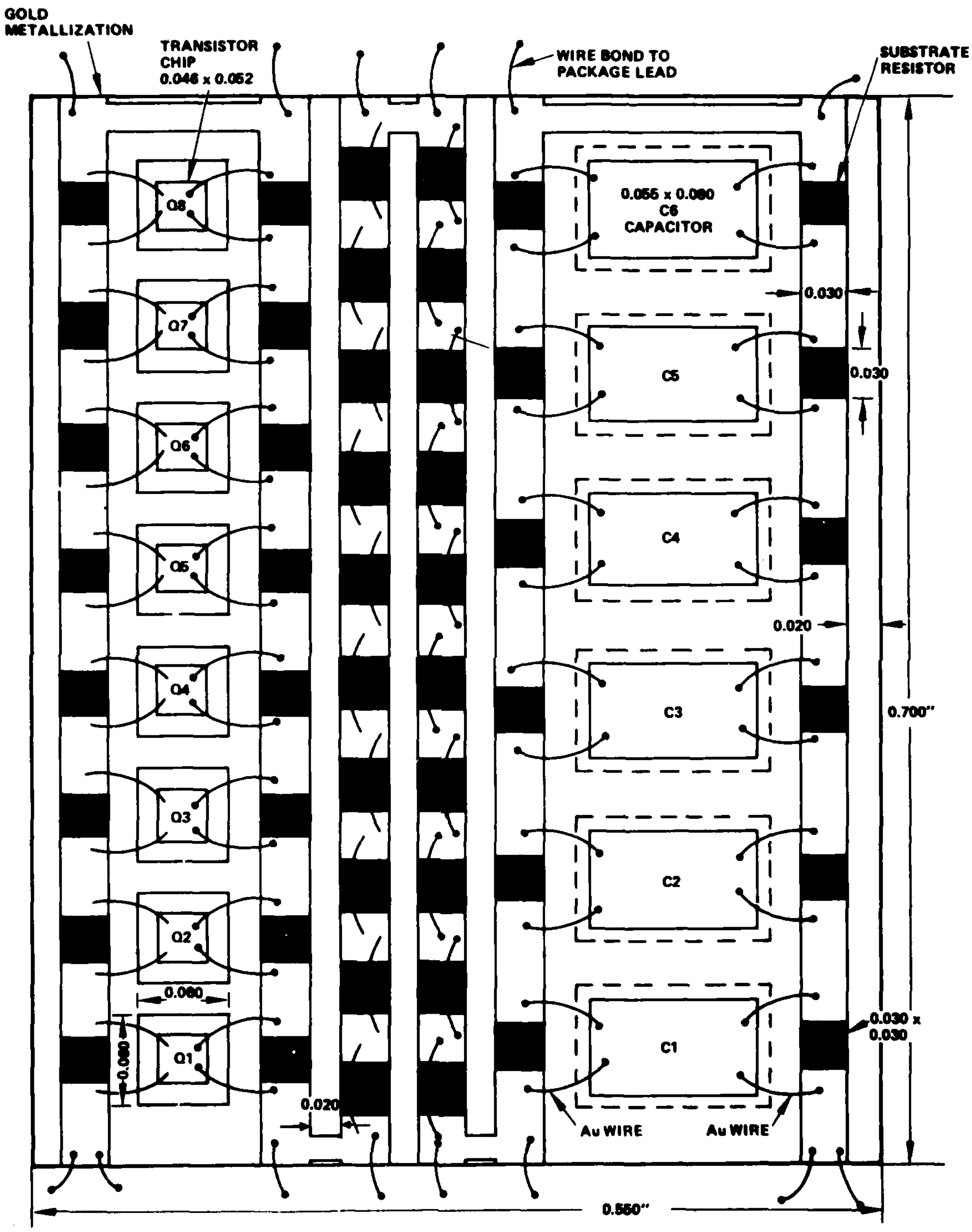


Figure 5. Layout of thick and thin film test specimen substrate.

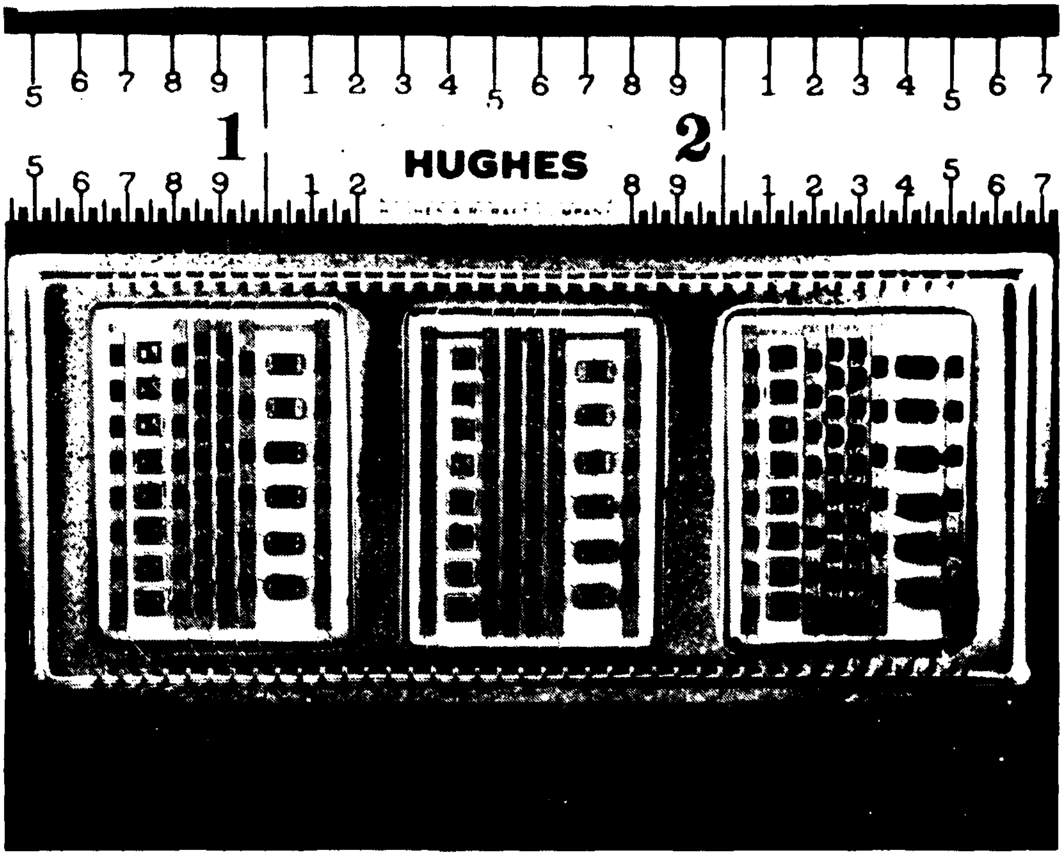


Figure 6. As assembled test hybrid, thick film substrates in a 1 x 2.3 inch metal package.

5.2 Test plan. The general test plan for rework procedures is schematically shown in Figure 8. This figure is an illustration of the fact that the evaluation of the test specimen integrates all the tasks of the program. The details of the test program are outlined in Figures 9, 10 and 11. The test hybrids were divided into three test sequence groups, each of which was subjected to a different sequence of repairs and tests. Table 10 shows all the combinations of conditions and the number of hybrids tested by the test program.

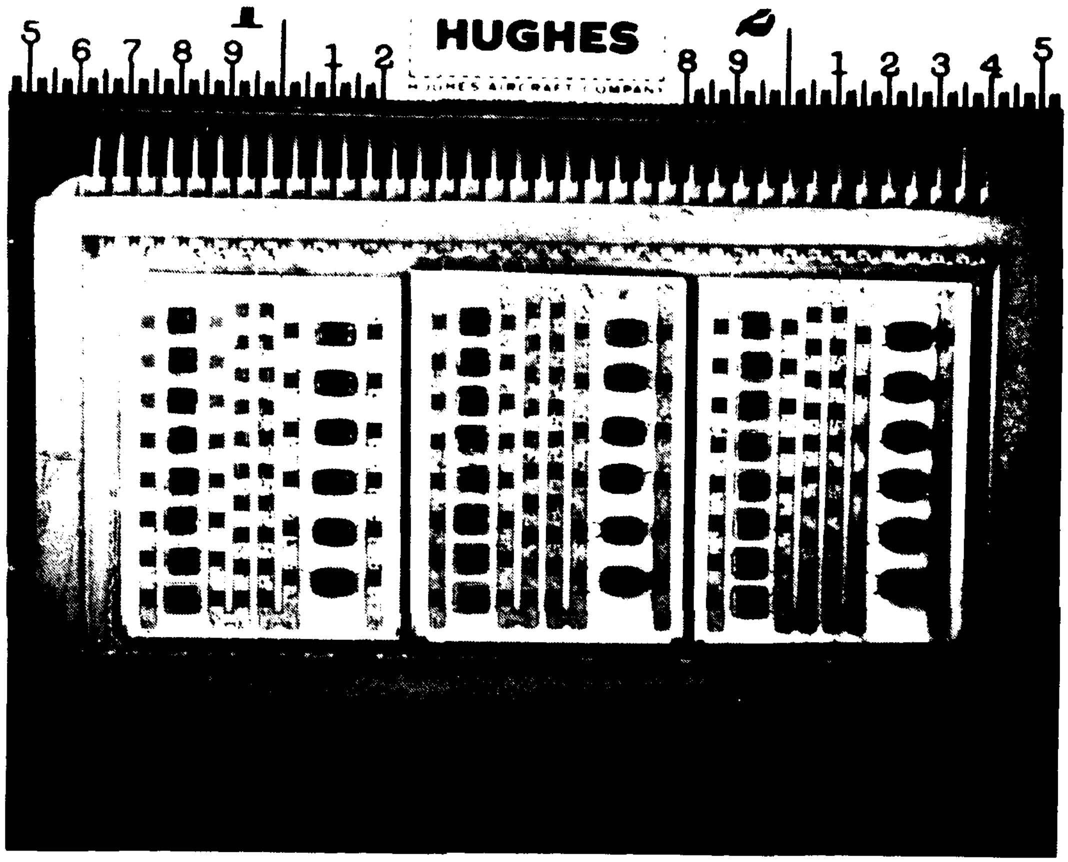


Figure 7. As assembled test hybrid, thin film substrates in a 1 x 2 inch ceramic base package.

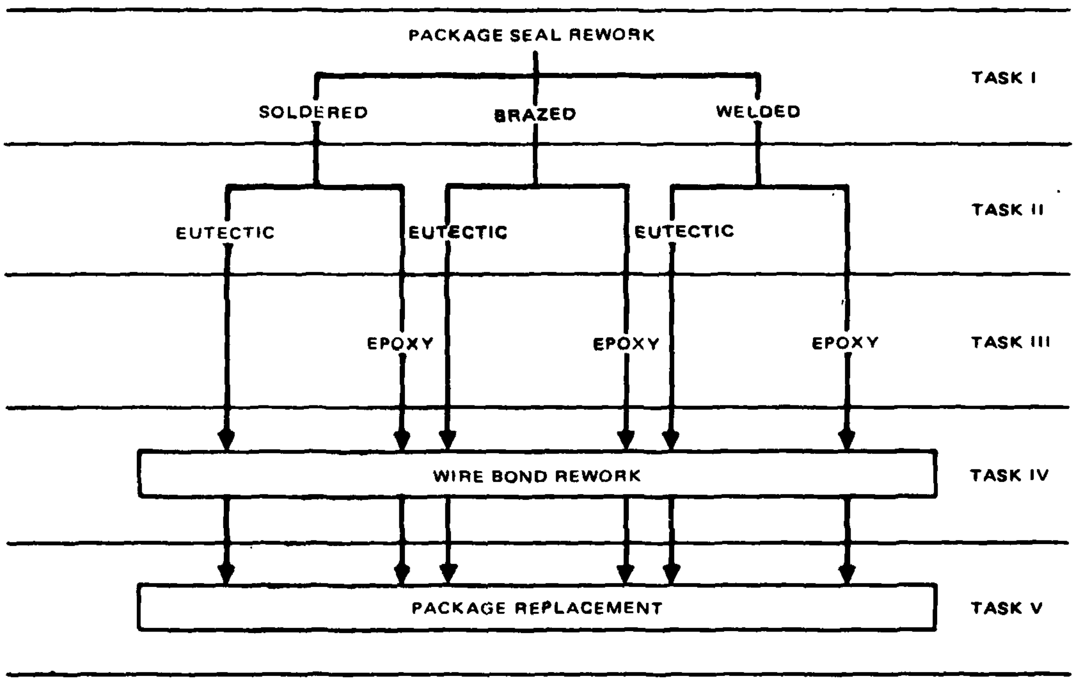
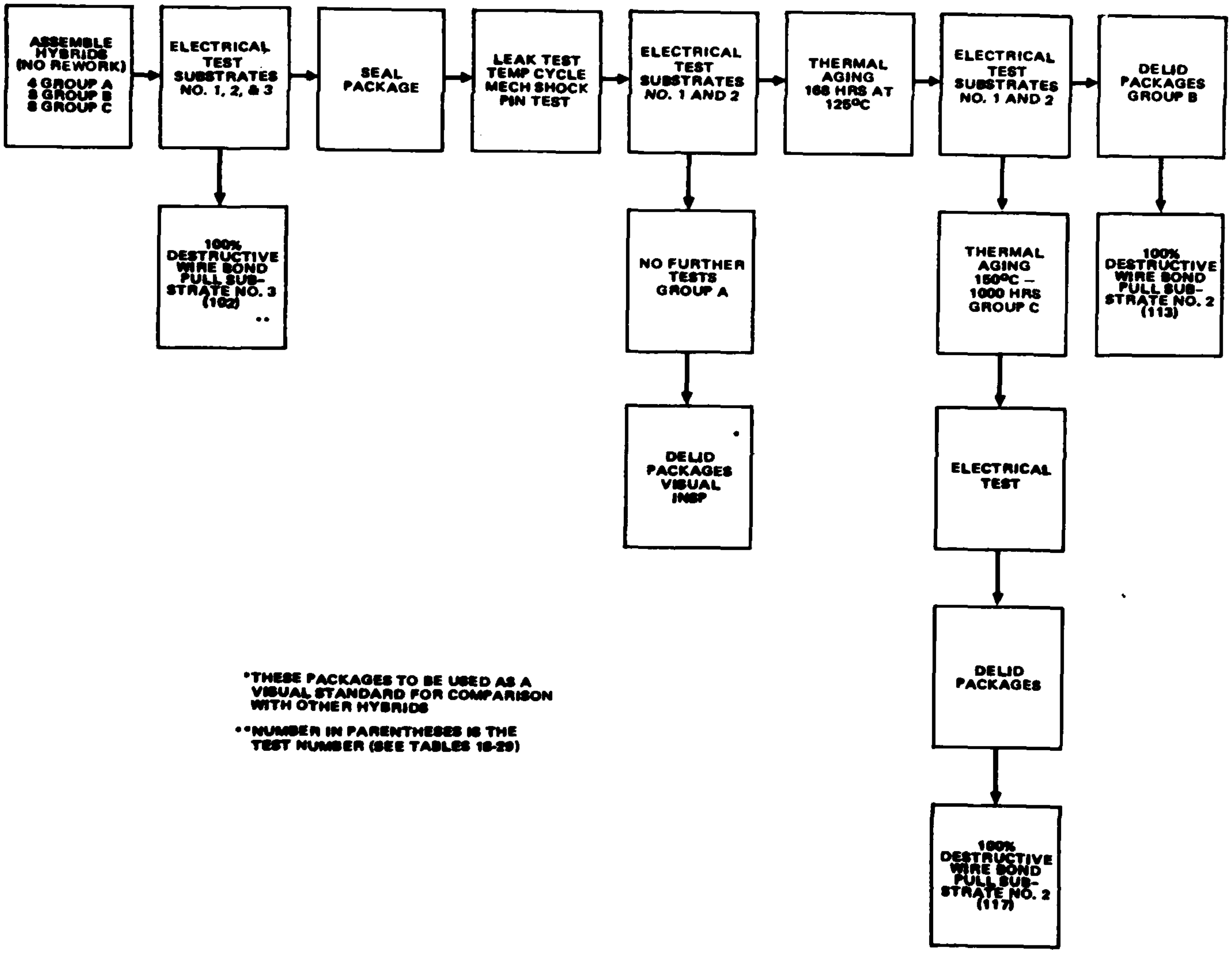


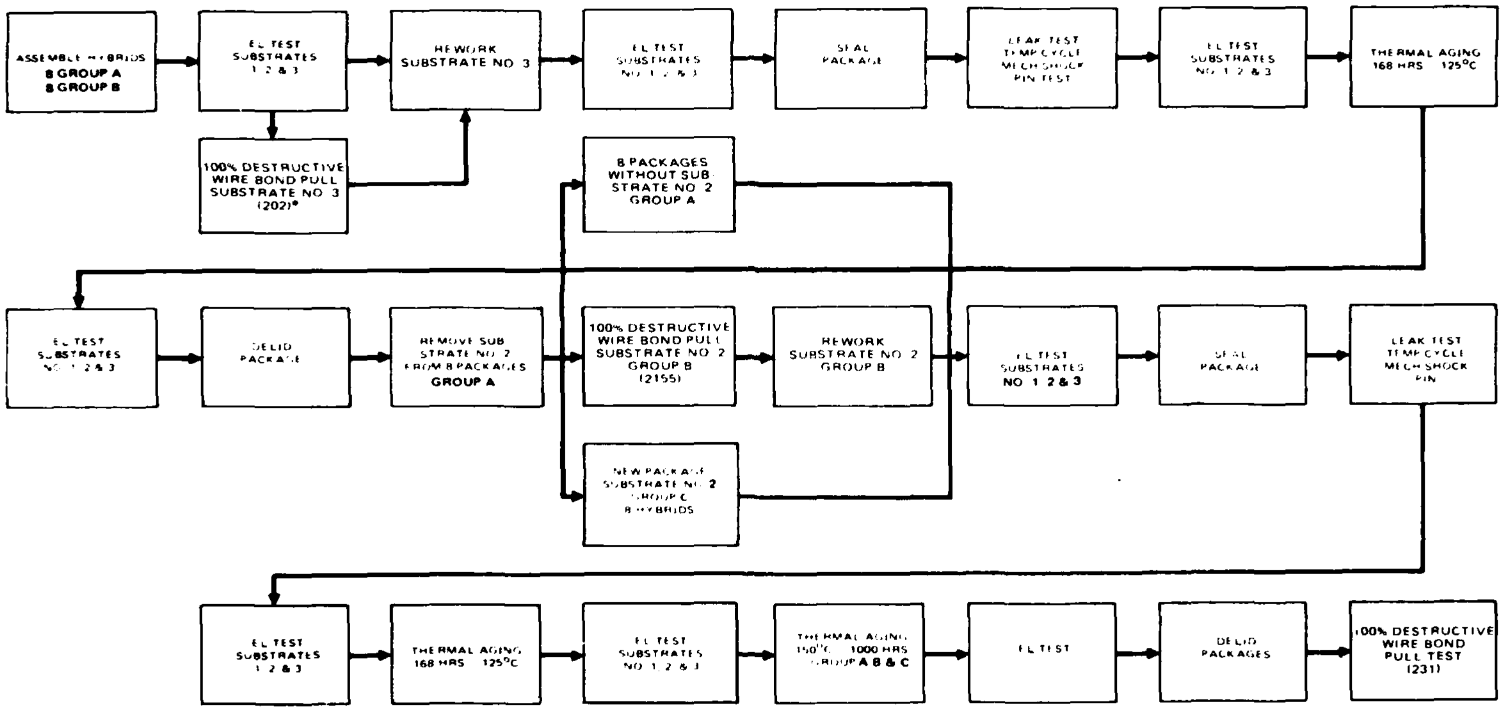
Figure 8. **Hybrid rework test programs**



*THESE PACKAGES TO BE USED AS A VISUAL STANDARD FOR COMPARISON WITH OTHER HYBRIDS

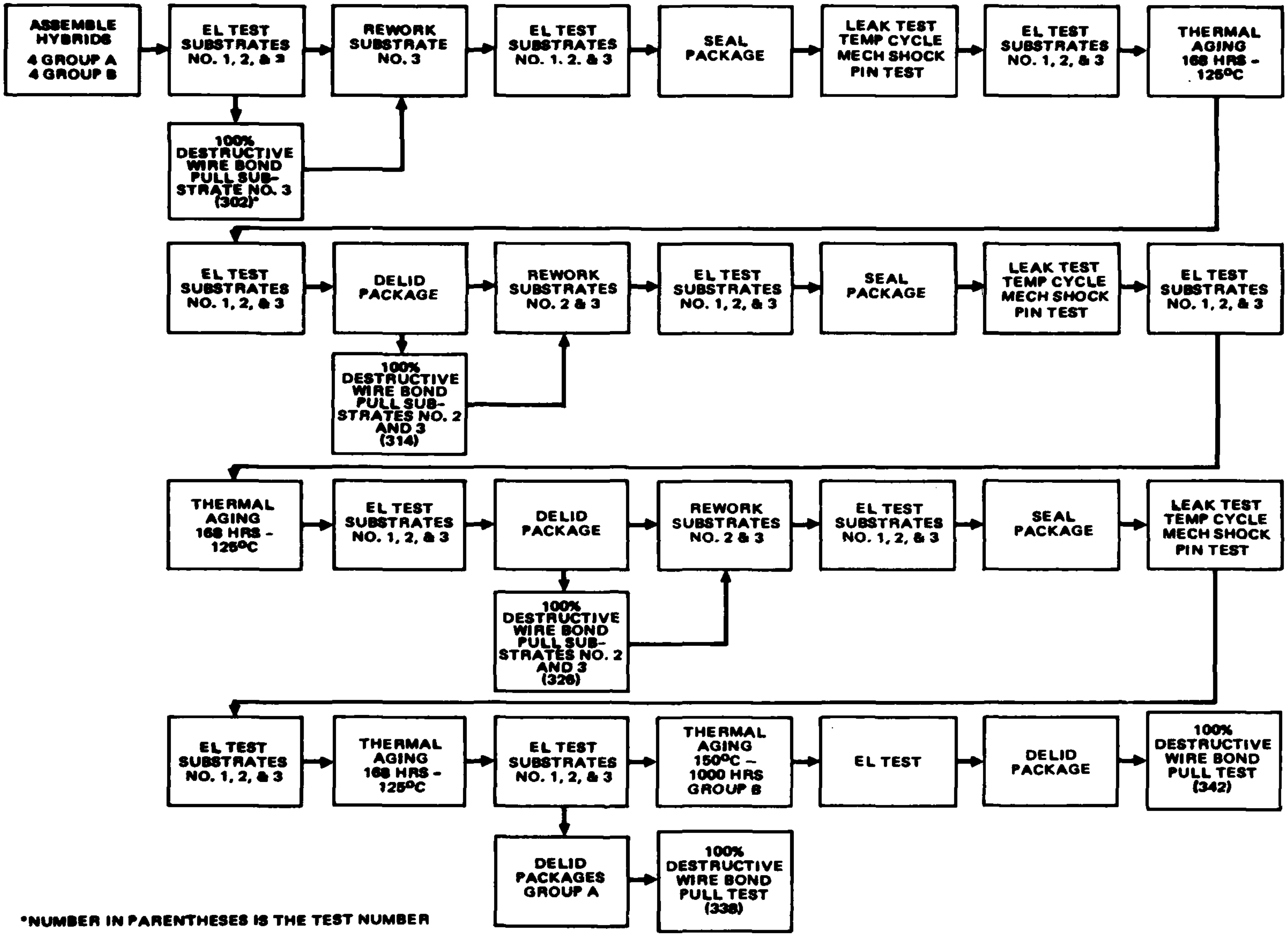
**NUMBER IN PARENTHESES IS THE TEST NUMBER (SEE TABLES 18-29)

Figure 9. Hybrid assembly flow diagram for sequence no. 1 -- (controls -- no rework)



*NUMBER IN PARENTHESES IS THE TEST NUMBER

Figure 10. Test hybrid assembly flow diagram for sequence no. 2 (one preseal rework, one postseal rework and one package replacement)



*NUMBER IN PARENTHESES IS THE TEST NUMBER

Figure 11. Test hybrid assembly flow diagram for sequence no. 3 (one preseal rework and two postseal reworks)

TABLE 10. TABULATION OF ALL CONDITIONS TO BE TESTED BY PERFORMING SEQUENCES 1, 2 AND 3 (FIGURES 10, 11 AND 12)

Table 13. Tabulation of all conditions to be tested by performing sequences 1, 2 and 3 (Figures 5, 6 and 7).

Hybrid Construction	Sequence 1 – Control Hybrids (20 hybrids)			Sequence 2 (24 hybrids)			Sequence 3 (8 hybrids)	
	Group A As Assembled (4)	Group B Delidded After Environmental Tests (8)	Group C Delidded After High Temperature Storage (8)	Group A Delidded One Substrate Removed After High Temperature Storage (8)	Group B Delidded After High Temperature Storage (8)	Group C New Package to House Removed Substrates Delidded After High Temperature Storage (8)	Group A Delidded After Environmental Tests (4)	Group B Delidded After High Temperature Storage (4)
Soldered Lid Thick Film Substrate Eutectic Attach	O	X	X	X	X	X	O	O
Soldered Lid Thin Film Substrate Eutectic Attach	O	X	X	X	X	X	O	O
Soldered Lid Thick Film Substrate Epoxy Attach	X	X	X	X	X	X**	X	X
Soldered Lid Thin Film Substrate Epoxy Attach†	X	X	X	X	X	X	X	X
Brazed Lid Thick Film Substrate Eutectic Attach	O	X	X	X	X	X	O	O
Brazed Lid Thin Film Substrate Eutectic Attach	O	X	X	X	X	X	O	O
Welded Lid Thick Film Substrate Epoxy Attach	X	X	X	X	X	X	X	X
Welded Lid Thin Film Substrate Epoxy Attach†	X	X	X	X	X	X	X	X

X = Condition tested
O = Condition not tested
† Ablefilm 550K for substrate attachment
*One substrate in each package – all others have three substrates per package.
**Planned but not performed.

Test sequence number 1 (Figure 9) consisted of test specimens which served as controls for the experiment. These 20 hybrids were not repaired, but were subjected to the standard environmental sequence that other specimens experienced. It was subdivided into Group A, B and C which served to provide data on wire bond changes as the environment test sequence proceeded.

Test sequence number 2 (Figure 10) evaluated the effects of one preseal repair and one postseal repair of parts, including the removal of one of the substrates in the package and its placement into a new package. This group started with 16 hybrids. Eight new hybrids (Group C) were formed when a substrate was removed from each of the 8 group A packages and placed in new packages. Test Sequence No. 2 has been structured to permit determination of the separate effects of (a) one package replacement and (b) one die and wire bond replacement after original package delidding. All three types of package sealing methods, all three types of substrate attachment methods and two types of chip attachment methods were included in Test Sequence No. 2.

Test Sequence No. 3, presented in Figure 11, consisted of 8 hybrids and evaluated the result of multiple reworks (one preseal and two postseal). The substrate and device attachment methods in this test sequence were limited to the polymeric (epoxy) technique. Package sealing methods included soft soldering and seam welding, but not seam brazing.

5.3 Test methods. Test methods are described as follows:

A. Electrical Test — A special test fixture was used in numerous electrical measurements to minimize the damage to the package lead wires or the metal/glass seal beads. The resistance of each row, corresponding to each type of wire bond on a given substrate, was measured. Each loose wire bond would cause the resistance to increase by 100 ohms. When the resistance increase was less than 100 ohms, probe measurements were made after the next delidding operation to determine the number of loops, or pairs of loops, (from wire bonds on devices) that showed an increase in bond electrical resistance.

B. Wire Bond Pull Tests — Non-destructive wire bond pull tests were made on all initial and reworked wire bonds to eliminate those which were marginal. Wire loops were pulled at 1 gm for 1 mil gold or aluminum wire and 3 gm for 2 mil gold wires. For the destructive pull test, wire loops were pulled to destruction with both pull strength and failure mode recorded. The failure modes are defined below:

N1 = failed at the neck of the first bond

N2 = failed at the neck of the second bond

W = wire broke

B1 = failed at the wire/metalization interface of the first bond

B2 = failed at the wire/metallization interface of the second bond

M1 = metallization lifted at the first bond

M2 = metallization lifted at the second bond

C. Leak Test – Both helium fine and fluorocarbon gross leak tests were performed per MIL-STD-883B, Method 1014.2, Conditions A and C.

D. Temperature Cycling Test – Temperature cycling was performed per MIL-STD-883B, Method 1012.2, Condition C (-65° to 150°C, 10 cycles).

E. Mechanical Shock Test – Mechanical shock testing was performed per MIL-STD-883B, Method 2002.2, Condition B (1500G, 5 shocks).

F. PIND Test – Particle impact noise testing was performed per MIL-STD-883, Method 2020, Condition B.

G. Thermal Aging Test – Thermal aging testing was carried out in an air circulated oven at 125°C for 168 hours. High temperature storage test was done at 150°C for 1000 hours.

5.4 Package sealing rework procedures.

5.4.1 Package sealing procedures. In this program, all ceramic packages were sealed by hand soldering (Sn10 solder). The metal packages were sealed by seam welding or by seam brazing using 80 gold/20 tin preforms. All package sealing was performed in a dry nitrogen atmosphere with a dew point of -55°C.

Prior to sealing, packages were cleaned and inspected. The cleaning process consisted of: a) rinse in methyl alcohol for 2 minutes, b) degrease in Freon TF vapor, c) Freon spray. The pretinned sealing surface of the ceramic package was cleaned with liquid trichloroethane prior to normal cleaning procedures. Lids and preforms were cleaned with trichloroethane and Freon TF.

5.4.2 Delidding procedures. Solder sealed packages were delidded thermally by immersing the lid, with package inverted, in a molten solder pot at 350°C. The sealing surfaces were retinned and cleaned with trichloroethane. Care was exercised to minimize the flux contamination inside the package.

Braze sealed packages were delidded mechanically using an Exactoknife. Welded packages were deliddng using a Hughes-designed milling machine. Metal package sealing surfaces were sanded to provide smooth surface for resealing. Particulate contamination was removed using low pressure nitrogen followed by alcohol and Freon rinses.

5.5 Eutectic attachment rework. The eutectic device attachment rework experiment consisted of bonding a silicon power transistor (Motorola MJEC 200) chip to a molybdenum tab using a gold-silicon eutectic alloy preform, followed by soldering the "moly" tab-chip assembly to the substrate.

The silicon chip had dimensions of 0.046 inch x 0.052 inch x 0.010 inch in thickness. All transistor chips were from a single lot.

The bonding pad metallizations for both thick film and thin film substrates were suitable for soldering. Bonding pad dimensions were 0.060 inch x 0.060 inch. Table 11 summarizes the metallization compositions, dimensions and sources of all materials used in evaluation of eutectic attachment rework.

A total of 384 chips were metallurgically bonded to the substrates. Of these chips, sixty-four were subjected to preseal rework and twenty-four were subjected to post seal rework. A summary of substrates and chip eutectically attached and reworked is presented in Table 12.

TABLE 11. SPECIFICATIONS OF MATERIALS AND COMPONENTS USED FOR EUTECTIC ATTACHMENT REWORK1/

Component or Material	Component or Material				
	Dimensions	Composition3/	Source	Front Metallization	Back Metallization
Transistor Chip	0.046x 0.052x 0.010		Motorola	Al	Au
Au-Si Preform	0.025x 0.025x 0.002	96.6 Au/3.1 Si 0.3 Ga	Cominco American Inc.		
Molybdenum Tab	0.055x 0.055x 0.005		Cominco American Inc.	Au, 99.9%, (0.0005 thick)	Au, 99.9%, (0.0005 thick)
Soft Solder		62 Sn/36 Pb/ 2Ag	Kester Solder Co		
Thin Film Substrate	0.55x 0.70x 0.025		Hughes Aircraft Company	Au/Ni/Au/ Nichrome2/	Au/Ni/Au/ Nichrome2/
Gold-tin Preform	0.55x 0.70x 0.002	80 Au/20 Sn	Cominco American Inc.		
Ceramic Package	1 x 2		3M Co.	Au/Ni (0.000125/0.00015)	
Metal Package	1x2.3		Tekform Products Co.	Au/Ni (0.00005-0.0001)/ (0.000005-0.00002)	
Thick Film Substrate	0.55x 0.70x 0.025		Hughes Aircraft Company	Pt/Au (ESL5800B)	Pt/Au (ESL5800B)

1/ All dimensions are in inches unless otherwise noted.
2/ Film thicknesses: 0.00025/0.000040/0.000010/350 A.
3/ Alloy compositions are in percent by weight.

AD-A092 950   HUGHES AIRCRAFT CO CULVER CITY CA MICROELECTRONIC PR--ETC F/G 9/5
HYBRID MICROCIRCUIT REWORK PROCEDURES EVALUATION.(U)
AUG 80 G T MALLOY   F30602-78-C-0310

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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

TABLE 12. PACKAGE TYPE AND SUBSTRATE TYPE COMBINATIONS EVALUATED IN EUTECTIC CHIP AND SUBSTRATE ATTACHMENT REWORK TESTS

		Chip Attachment			Substrate Attachment	
Package Type	Substrate Type	No. of Chips Attached	No. of Chips Preseal Reworked	No. of Chips Post Seal Reworked	No. of Substrates Attached	No. of Substrates Remounted
Metal	Thick Film	96	16	8	12	1
Metal	Thin Film	96	16	8	12	1
Ceramic	Thick Film	96	16	0	12	1
Ceramic	Thin Film	96	16	0	12	1
Totals		384	64	16	48	4

5.5.1 Chip attachment procedures. Both chip-to-molytab attachment and molytab-to-substrate attachment were carried out manually on a heated stage, under a 30x microscope in an ambient room atmosphere. The temperature of the hot stage was monitored by a surface thermometer.

A. Chip-molytab attachment: All parts were cleaned with acetone then a gold-silicon preform was placed between the chip and the molytab. The assembly was carefully placed on a heated stage preheated to 400°C. Once the preform started to melt, the chip was lightly scrubbed and pressed with a pair of tweezers while the molytab was held in place with another pair of tweezers. The assembly was then removed from the stage and allowed to cool. No flux was used. The assembly was visually inspected at 30x magnification for defects. Parts with improper alignments, tilting, fillet less than 75 percent of the periphery of the die or poor wetting were rejected to the requirements of MIL-STD-883B.

B. Molytab-substrate attachment: Both molytab and substrate metallization pads were pretinned with Sn 62 solder prior to reflow attachment. Tinning of the substrate metallization was done using a soldering iron on a hot plate heated to 100°C. Care was exercised not to damage the nearby gold conductor. The thickness of the solder coating was kept to a minimum. The back side of the molytab was tinned by scrubbing it over a thin layer of molten solder on top of a flat sheet of copper. Reflow attachment was carried out at 190°C. It was necessary to add a small amount of solder to the pad just before reflow attachment to improve the quality of the metallurgical bonds. Kester No. 197 mild rosin flux was used during the tinning and reflow processes. The substrate was finally cleaned with methyl alcohol and acetone.

5.5.2 Chip attachment rework procedures. Chip attachment rework consisted of removal of the moly tab-chip assembly from the substrate and reattachment of a new moly tab-mounted transistor chip to the substrate, using Sn62 solder (M. P. = 183°C) to bond the tab to the substrate as described below.

A. Preseal Rework — Most of the moly tabs were detached from the substrates using a Semiconductor Equipment Corporation Model No. 4400 "Hot Gas Die Remover." This equipment provides sufficient hot air (or nitrogen) to heat locally to well above 300°C. A total of fourteen chips, out of sixty-four which could not be removed using the hot gas die remover system, were mechanically pushed off their substrates (held at 150°C in air) using a small chisel. Almost all of the solder alloy compositional changes had occurred as a result of oxidation and solder leaching. The solder pads could not be remelted at 200°C, but became rebondable after repeated addition and removal of fresh solder. Visually, the quality of the bonding was considered to be inferior.

B. Postseal Rework — All moly tab-mounted chips were mechanically pushed off the substrate since they could not be removed by the hot gas jet technique. Rebonding of new moly tab-mounted transistor chips was performed using the aforementioned preseal rework technique. Solder leaching occurred on some of the bonding pads.

In general, it was found that reworking of eutectically attached devices and substrates was found to be very difficult, and, in some cases, very destructive.

5.6 Polymer attachment rework. Two types of device attachment were performed in this program. They are:

(1) Bonding a silicon chip device to the substrate using silver conductive epoxy Ablebond 606-2.

(2) Bonding a chip ceramic capacitor to the substrate using nonconductive epoxy Scotchcast 281.

The same silicon chip device as described in eutectic attachment was used for polymer attachment rework. The capacitor had a dimension of 0.055 x 0.080 x 0.050 inches, was terminated with a silver/palladium (80/20) metallization. Each capacitor was electrically checked for shorts prior to attachment. Capacitors were purchased from U.S.C.C. Centralab, Johnson Control Inc.

A total of 672 silicon chips and 504 capacitors were polymerically attached to the substrates. Using polymeric material (epoxy), 416 silicon chips and 312 capacitors were reworked. A breakdown of substrate and package types used is given in Table 13.

5.6.1 Device attachment procedure. To attach a silicon chip onto the substrate, a thin layer of epoxy was first applied to the bonding area. The chip was then scrubbed in place lightly until epoxy could be seen at all four corners of the device. The epoxy was subsequently cured at 125°C for two hours. Similar procedures were used to bond capacitors to substrates except the epoxy was air-dried for 2-4 hours before curing to minimize the bleed out.

5.6.2 Device attachment rework procedure. Both silicon chips and capacitors were removed from the substrate using a hot gas die remover (Semiconductor Equipment Corp. Model No. 4400). Residual epoxy on the substrate was carefully removed using a small tool and isopropyl alcohol. Loose particles were blown off the substrate with low pressure nitrogen.

Procedures employed for attaching new chips and capacitors to the substrate were the same as described above.

5.7 Interconnection repairs. Interconnection rework consisted of:

(1) Chip-to-substrate — 1 mil aluminum wire, ultrasonic

(2) Chip-to-substrate — 1 mil gold wire, thermosonic

(3) Substrate-to-substrate — 1 mil aluminum wire, ultrasonic

(4) Substrate-to-substrate — 2 mil gold, thermocompression

(5) Substrate-to-capacitor — 2 mil gold, thermocompression

Typical wire bonds are shown in Figures 12, 13 and 14.

In order to maintain the quality as well as the uniformity of wire bond processing, the performance of each bonder was monitored at 4 hour intervals by conducting a destructive wire pull test on special specimens.

TABLE 13. SUMMARY OF DEVICES AND SUBSTRATES POLYMER ATTACHED TO VARIOUS PACKAGES AND SUBSTRATE TYPES

		Chip Attachment				Capacitor Attachment				Substrate Attachment	
Package Type	Substrate Type	No. of Chips Attached	No. of Chips Preseal Reworked	No. of Chips 1st Post Seal Reworked	No. of Chips 2nd Post Seal Reworked	No. of Capacitors Attached	No. of Capacitors Preseal Reworked	No of Capacitors 1st Post Seal Reworked	No. of Capacitors 2nd Post Seal Reworked	No. of Substrates Attached	No. of Substrates Re-Attached
Metal	Thick film	168	32	40	32	126	24	30	24	21	1
Metal	Thin film	168	32	40	32	126	24	30	24	21	1
Ceramic	Thick film	168	32	40	32	126	24	30	24	21	0
Ceramic	Thin film	168	32	40	32	126	24	30	24	21	1
Totals		672	128	160	128	504	96	120	96	84	3

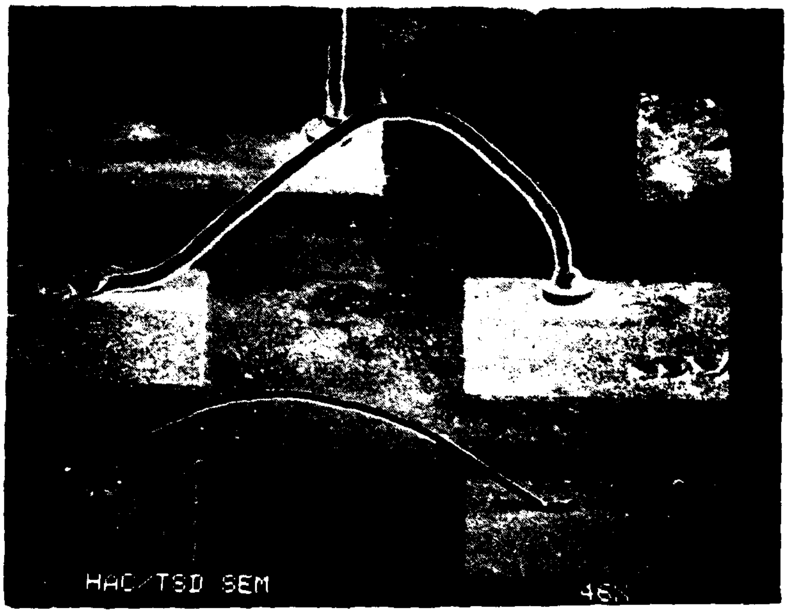

Figure 12. Substrate to substrate wire bonds, lower: 1 mil aluminum, ultrasonic upper; 2 mil gold, thermocompression 39x.

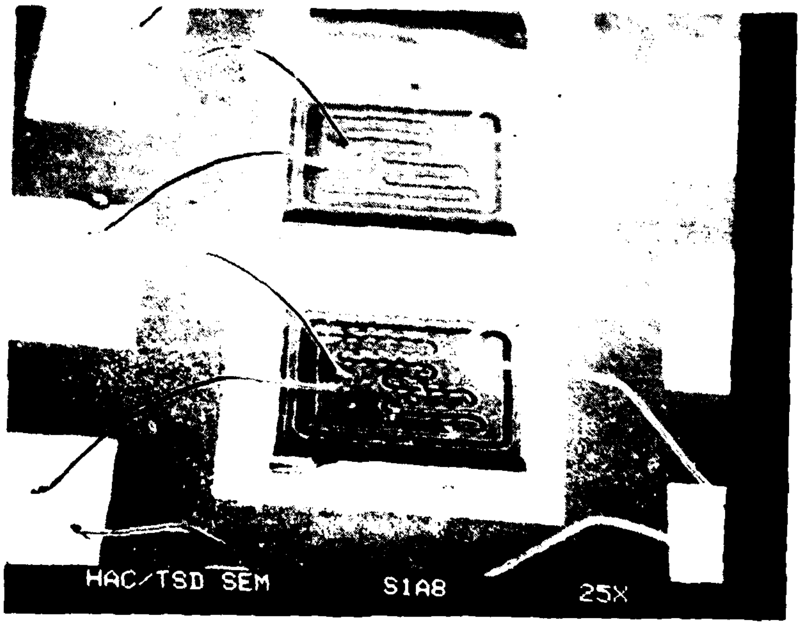

Figure 13. Chip to substrate wire bond left: 1 mil aluminum, ultrasonic right: 1 mil gold, thermosonic 25x.

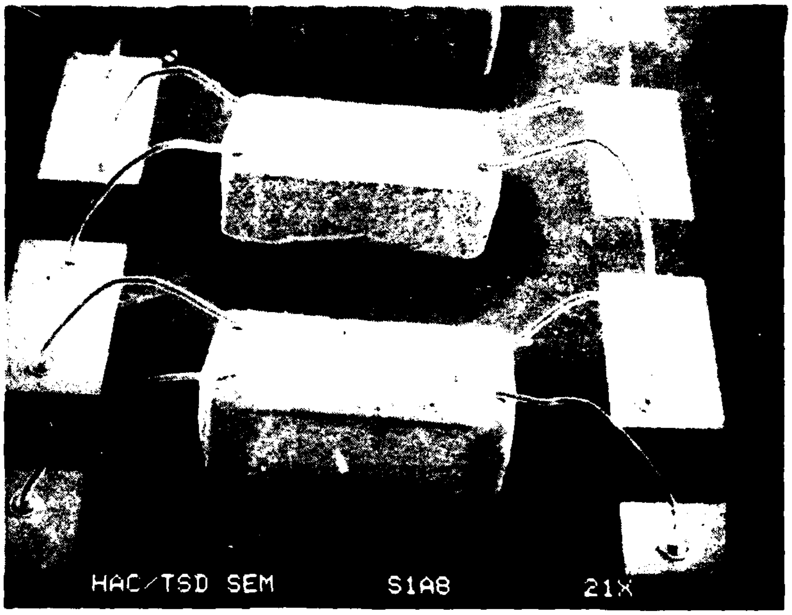

Figure 14. Substrate to capacitor wire bonds, 2 mil gold thermocompression 21x.

Bonding machine parameters were then adjusted as indicated by the pull test results. In addition, to minimize variations due to use of different operators on a given wire bonding process, one operator was assigned to each of the three bonding methods employed. A total of three operators was used throughout the program.

To ensure that all wire bonds were good, a 100 percent nondestructive wire bond pull test was implemented using a force of 1 gram for 1 mil diameter gold and aluminum wires and a force of 3 grams for the 2 mil diameter gold wires.

5.8 Substrate attachment rework. Substrate attachment rework consisted of eutectic attachment and polymer attachment. All substrates for eutectic chip attachment were affixed eutectically to package bases using gold-tin hard solder. Substrates for polymer chip attachment were epoxy bonded to the package bases. Two types of non-conductive polymer were used for substrate attachment: Scotchcast 281 paste for thick film and Ablefilm 550K preforms for thin film substrates. A total of 132 substrates, 48 eutectic and 84 polymer, was attached to the 44 packages each of which contained three identical substrates. Seven substrates were removed and placed in new packages.

5.8.1 Substrate attachment procedures.

A. Eutectic attachment – The procedure used to attach the substrate to the package base was as follows:

(a) Substrates were attached to a package base by reflowing a gold-tin preform (M.P. 280°C), 0.55 x 0.70 x 0.002 inches, at 300°C.

(b) Each package was preheated to 125°C, before placing it on the high temperature stage for reflow bonding, to prevent cracking the ceramic package base or glass beads of the metal package. After bonding, the package was cooled, then cleaned with trichloroethane.

Substrate attachment was performed after chips and capacitors were already mounted on the substrate. This sequence was adopted to minimize prolonged exposure of the three substrates, in a given package, to the high temperature of eutectic chip attachment.

B. Polymer attachment – Attachment using Scotchcast 281, was made by applying a thin epoxy coating to the package bonding surface followed by light pressing of the substrate to form a void-free bond. When Ablefilm 550K was used, it was presoftened at 125°C. The curing process was applied for 2 hours at 125°C for both materials.

5.8.2 Substrate rework procedures.

A. Eutectic attachment rework – Substrates were removed from the package by heating at 300°C. The procedure used to attach the substrate to a new package was the same as that described in Section 5.8.1. Care was exercised to avoid mechanical damage to the devices and interconnections on the substrate.

B. Polymer attachment rework — The substrates were removed by heating the package at 150°C. The procedure used to attach the substrate to a new package was the same as that described in Section 5.8.1. Three substrates were removed and attached to the new packages.

6.0 TASK I. PACKAGE SEALING REWORK

6.1 Objectives. The purpose of this task was to evaluate and compare three commonly used methods for sealing hybrid microcircuit packages: seam welding, hard solder ("braze") sealing and soft solder sealing.

A secondary goal of this task was to ascertain the number of times a welded or soldered package could be delidded or resealed before degradation of the components or package seal was detected. An assessment of the effect of the delidding and resealing processes on hybrid reliability was made. Particular attention was given to the effect of thermal stress on package seal integrity.

6.2 Test results. The leak test results on all packages are summarized in Table 14. These results were the leak rate values after the final sealing operation; some packages that failed in the first sealing attempt were allowed one touch up seal.

Most ceramic packages using soft solder (Sn10) sealing can be resealed at least two times with no increase in the measured leak rate. The inability to reseal three packages, which contained eutectically attached substrates, was caused by thermal stress - induced cracking of the package bases during previous device attachment rework.

All of the packages resealed by seam brazing were gross leakers. These results are in general agreement with those of previous programs.(1)

Seam welded metal packages could be resealed successfully. However, some packages showed a deterioration in hermeticity with increased reseals, presumably due to glass bead cracking.

6.3 Significance of results.

- The seal integrity of soft solder-sealed packages, containing eutectically attached substrates and devices, can be degraded if the package is thermally stressed during the device rework process.
- The seal integrity of soft solder-sealed packages, containing epoxy attached substrates and devices, is not degraded during the device/substrate rework process.

TABLE 14. EFFECT OF REWORK ON PACKAGE HERMETICITY

Package No.	Package Type	Sealing Method	First Seal Fine Leak	First Seal Gross Leak	First Reseal Fine Leak	First Reseal Gross Leak	Second Reseal Fine Leak	Second Reseal Gross Leak
S1A3	Ceramic	SN10	1.4×10^{-8}	P				
A4			1.2×10^{-8}	P				
B1			1.8×10^{-8}	P				
B2			1.5×10^{-8}	P				
B3			1.2×10^{-8}	P				
B4			1.4×10^{-8}	P				
C1			1.0×10^{-8}	P				
C2			1.2×10^{-8}	P				
C3			1.6×10^{-8}	P				
C4			1.0×10^{-8}	P				
S2A1			4.8×10^{-8}	P	1.0×10^{-9}	P		
A2			6.4×10^{-9}	P	F (1)	F		
A3			1.0×10^{-9}	P	1.0×10^{-9}	P		
A4			4.0×10^{-9}	P	1.6×10^{-9}	P		
B1			3.4×10^{-9}	P	– (2)	–		
B2			1.6×10^{-8}	P	– (2)	–		
B3			1.0×10^{-9}	P	2.6×10^{-9}	P		
B4			4.8×10^{-9}	P	0.8×10^{-9}	P		
C1			1.6×10^{-8}	P				
C2			2.0×10^{-8}	P				
C3			– (3)	–				
C4			1.4×10^{-8}	P				
S3A3			1.0×10^{-9}	P	1.8×10^{-9}	P	0.6×10^{-9}	P
A4			1.0×10^{-9}	P	1.0×10^{-9}	P	0.4×10^{-9}	P
B3			1.0×10^{-9}	P	1.0×10^{-9}	P	1.2×10^{-9}	P
B4			1.0×10^{-9}	P	4.2×10^{-9}	P	1.2×10^{-9}	P
	Yield		21/21		9/12			

(1) Package cracked during resealing

(2) Not sealed, packages cracked during delidding

(3) Not sealed

P - Passed

F - Failed

(Table 14, Continued)

Package No.	Package Type	Sealing Method	First Seal Fine Leak	First Seal Gross Leak	First Reseal Fine Leak	First Reseal Gross Leak	Second Reseal Fine Leak	Second Reseal Gross Leak
S1B5	Metal	Seam Braze	1.0×10^{-7}	P				
B6			4.0×10^{-8}	P				
C5			4.8×10^{-8}	P				
C6			4.2×10^{-8}	P				
S2A5			3.2×10^{-8}	P	F	F		
A6			1.0×10^{-7}	P	F	F		
B5			4.0×10^{-8}	P	F	F		
B6			3.0×10^{-8}	P	F	F		
C5			6.0×10^{-8}	P				
C6			3.6×10^{-8}	P				
S1A7		Seam Weld	2.6×10^{-8}	P				
A8			3.4×10^{-8}	P				
B7			4.4×10^{-8}	P				
B8			6.0×10^{-8}	P				
C7			4.6×10^{-8}	P				
C8			5.0×10^{-8}	P				
S2A7			F	P	F	P		
A8			F	P	F	P		
B7			2.6×10^{-8}	P	F	P		
B8			3.2×10^{-8}	P	4.2×10^{-7} F	P		
C7			5.4×10^{-8}	P				
C8			6.2×10^{-8}	P				
S3A7			1.4×10^{-8}	P	F	P	F	F
A8			1.3×10^{-8}	P	2.6×10^{-8}	P	2.6×10^{-7}	P
B7			1.6×10^{-8}	P	2.6×10^{-8}	P	2.6×10^{-7}	P
B8			1.1×10^{-8}	P	F	P	F	P
Seam Braze Yield			10/10		0/4			
Seam Weld Yield			14/16		2/8		0/4	

- Packages sealed by seam brazing can not be resealed with a high resealing yield.
- Seam weld package sealing rework is a viable process, although glass bead cracking during the rework process caused degradation in package hermeticity. This conclusion should be tempered by the fact that the packages used for this test program have 80 glass-to-metal seals and are quite susceptible to thermal stress cracking of the glass beads. Hughes experience with other less sensitive packages has shown that seam welded packages can be resealed in excess of five times without failures.

7.0 TASK II. REWORK OF EUTECTICALLY ATTACHED DEVICES

7.1 Objectives. The objective of the eutectic device attachment rework task was to evaluate the effects of rework of metallurgically bonded chips on component and package reliability. A secondary objective of this evaluation was to determine the number of times a soft solder (Sn62) bonded,molytab-mounted chip could be reworked before solder bond degradation commenced.

7.2 Test results. Rework of eutectically attached silicon device chips was technically difficult for a circuit consisting of: gold conductors, devices that were both eutectically and polymerically bonded to the substrate and bimetallic wire bonds already on the circuit. This type of circuit limited the temperature that could be used for chip detachment as well as re-attachment.

Considerable difficulties were experienced in the rework process. Fourteen chips out of sixty-four in the preseal rework and all of the thirty-two chips in the post seal rework could not be removed using a hot gas die remover. These devices had to be mechanically pushed off their substrates (held at 150°C in air) using a small chisel. The causes are: (1) increased liquidus, or softening temperature of the solder alloy due to leaching of the conductor pad, (2) oxidation of solder, (3) complexity of the test specimen and (4) high temperature exposures during eutectic substrate attachment (300°C) and hybrid environmental tests (125°C and 150°C). With mechanical push-off, particulate contamination from chip breakage or cracking, and scratches of conductors commonly occurred. Practically all of the solder pads had a grained appearance. Upon heating to 200°C, the solder softened but was not able to form a bond with a new moly tab-mounted chip. Re-attachment of devices was accomplished only after repeated addition and removal of fresh solder. Solder leaching occurred on some of the bonding pads, mostly thick film. Flux removal became increasingly difficult with successive reworks since repeated heating of the substrate had caused the flux to harden.

7.3 Significant of results.

- Rework of solder bonded, moly tab-mounted chips is limited metallurgically as a result of solder oxidation and solder leaching. Although the silicon device chips may be bonded without the use of moly tabs, the reliability risks are increased due to the higher (>400°C) temperature required to detach the eutectically bonded chip from the gold metallization.
- There is a potential danger of fracturing the glass bead seals of metal packages, the substrate and the base of ceramic packages due to thermal shock.
- Damage to other components or devices already on the hybrid substrate is likely due to high rework process temperatures. The components and circuit elements most susceptible are epoxy adhesives and wire bonds.

8.0 TASK III. REWORK OF POLYMERICALLY ATTACHED DEVICES

8.1 Objectives. Although a large data base is available that supports the use of epoxy materials as a reliable process for the attachment of hybrid devices and substrates, the influence of specific rework procedures and the effects of repeated rework require further experimental evaluation. The purpose of the polymer attachment rework task was to assess the effects of attachment and rework of active and passive devices (using both conductive and non-conductive epoxies) on hybrid microcircuit reliability. Particular emphasis was placed on preventing chemical and particulate contamination of the various hybrid elements during assembly and rework of the test specimens.

8.2 Results. Rework of devices attached with epoxy was a relatively simple and an easy process compared with devices eutectically attached. Removal of silicon chips and capacitors was accomplished, without difficulty, using the "Hot Gas Die Remover." Device attachment rework caused no thermal damage to package base, substrate, devices or interconnections on the neighboring substrates.

Particle contamination due to fracturing of silicon chip or capacitor was practically non-existent during the device removal process. Contamination due to loose epoxy particles, during the residual epoxy removal process, could be avoided by careful practice, aided by a thorough visual inspection. A thin layer of epoxy contamination on conductors deposited during final solvent cleaning is a cause of concern because a contaminated surface will affect the bondability and reliability of subsequent wire bond interconnections. A minimum amount of the proper solvent (methyl alcohol) should be used and cleaning should be performed under a microscope.

Re-attachment of new devices onto the substrate poses no reliability risk if proper procedures are followed. The device-substrate bond quality was as good as that of initial bonds. There were no loose chips and capacitors after environmental test or high temperature storage.

8.3 Significance of results.

- Rework of polymer bonded devices does not influence the reliability of the hybrid. Due to low process temperatures involved, there is no detectable thermal damage to package, substrate, devices or interconnections already on the substrate.
- Particle contamination can be avoided with careful workmanship aided by a thorough visual inspection.
- Epoxy contamination deposited on substrate conductors during final solvent cleaning must be avoided to insure reliable wire bonds.

9.0 TASK IV. INTERCONNECTION REPAIRS

9.1 Objectives. The purpose of the interconnection rework task was to evaluate and compare three interconnect bonding processes presently employed in the fabrication of hybrid microcircuits: aluminum wire ultrasonic, gold wire thermosonic and gold wire pulsed thermocompression.

Using the bond pull strength and bond electrical resistance as the criteria for reliability, the quality of original and repaired gold and aluminum wires was determined (a) before and after environmental tests and high temperature storage (150°C, 1000 hours), (b) before and after package replacement, (c) before and after replacement of devices using both eutectic and polymer attachment methods.

9.2 Test results. The pull test and electrical test results of test sequences 1, 2 and 3 are summarized in Tables 15, 16, 17 and 18. The pull test data from packages that were non-hermetically sealed were included in the calculations since hermeticity did not appear to affect the pull strength. Five major wire bond failure modes, N1, N2, W, B1 and B2 are also defined.

The electrical test data comprise the number of loose wires detected during the environmental tests and the number of interconnections that developed bond electrical resistance increases. Each bond electrical resistance increase entered in the data tables represents the measured resistance for a wire loop, (or a pair of loops connecting devices), that is in excess of two times its normal resistance value. It should be pointed out that the majority of bond electrical resistance increases were in the order of a few tenths of an ohm, which would not be expected to affect the electrical performance of a hybrid microcircuit.

(1) Test No.	Substrate Type	Group	Chip and Substrate Attachment Method	Sub-strate No.	Chip-to-Substrate(2) 1 Mil Aluminum, Ultrasonic											
					N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$
102	Thick Film	B, C	Eutectic	3	64	4.3	1.6	7	55	0	1	1	0	0	64	6.
		A, B, C	Epoxy	3	96	5.7	1.3	34	61	0	1	0	0	0	96	6.
113	Thick Film	B	Eutectic	2	30	3.6	1.0	16	14	0	0	0	0	0	32	4.
			Epoxy	2	32	3.6	1.7	8	24	0	0	0	0	0	32	6.
117	Thick Film	C	Eutectic	2	32	2.4	0.9	0	31	0	1	0	0	0	32	4.
			Epoxy	2	32	3.4	1.2	14	17	0	0	0	0	0	32	6.
102	Thin Film	B, C	Eutectic	3	64	5.6	1.7	25	37	0	0	2	0	0	64	6.
		A, B, C	Epoxy	3	96	6.5	1.5	44	51	0	0	0	0	0	96	7.
113	Thin Film	B	Eutectic	2	32	2.4	1.5	5	14	0	0	13	1	5	30	5.
			Epoxy	2	32	4.9	0.9	20	12	0	0	0	0	0	32	7.
117	Thin Film	C	Eutectic	2	32	3.9	1.7	7	24	1	0	0	0	5	32	7.
			Epoxy	2	32	4.2	0.9	10	21	1	0	0	0	0	32	7.

(1) 102 = As wired; 113 = Environmental tested; 117 = High temperature storaged (150°C/

(2) N = Number of wire loops pulled; $\overline{X}$ = Average pull strength in grams; S = Standard dev second bond; W = Number of failures at the wire (wire broken); B1 = Number of failure loose wires; R = Number of wire loop(s) showing bond electrical resistance increase

1

TABLE 15. SUMMAR
TEST SE

Chip-to-Substrate 1 Mil Gold, Thermosonic									Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic										Substrate-to-Substra 2 Mil Gold, Thermocomp						
$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1
6.2	2.0	25	27	5	1	5	0	0	40	4.4	1.4	32	8	0	0	0	0	0	40	27.4	5.2	12	2	14	5
6.6	1.6	42	39	13	0	2	0	0	60	5.2	1.6	42	16	0	0	2	0	0	60	27.6	9.3	18	7	26	4
4.3	3.0	8	16	0	3	5	0	0	20	3.6	1.0	13	6	0	0	1	0	0	20	26.2	6.9	4	11	3	2
6.1	1.9	10	19	3	0	0	0	0	20	4.2	1.3	19	1	0	0	0	0	0	20	28.6	6.9	3	4	10	3
4.2	2.9	20	7	3	2	0	0	0	20	2.9	0.9	6	14	0	0	0	0	0	20	30.9	4.4	8	0	11	1
6.9	1.2	19	11	2	0	0	0	0	20	3.1	1.2	9	11	0	0	0	0	1	20	30.4	5.5	6	5	9	0
6.7	1.6	30	23	11	0	0	0	0	40	8.3	1.1	28	12	0	0	0	0	0	40	30.5	4.4	10	15	12	0
7.0	1.2	56	13	26	0	1	0	0	60	7.6	1.0	45	15	0	0	0	0	0	60	29.5	5.1	27	1	25	7
5.7	1.8	4	20	1	5	0	0	6	20	3.2	2.0	9	4	0	5	0	1	6	20	30.3	5.6	0	11	8	1
7.7	0.8	14	6	12	0	0	0	0	20	4.0	1.6	10	10	0	0	0	0	0	20	33.0	3.2	10	4	6	0
7.0	1.5	10	15	5	2	0	0	1	20	3.9	1.9	8	2	1	8	1	0	4	20	28.4	5.2	4	8	6	1
7.5	0.8	17	10	5	0	0	0	0	20	4.4	0.8	12	7	0	1	0	0	0	20	32.1	4.2	7	7	6	0

C/1000 hrs.)

leviation in grams; N1 = Number of failures at the neck of the first bond; N2 = Number of failures at the neck
ires at the first bond/wire interface; B2 = Number of failures at the second bond/wire interface; L = Number
e

TABLE 15. SUMMARY OF PULL TEST AND ELECTRICAL TEST RESULTS
TEST SEQUENCE 1 (NON-REWORKED, CONTROL)

to-Substrate um, Ultrasonic						Substrate-to-Substrate 2 Mil Gold, Thermocompression										Substrate-to-Capacitor 2 Mil Gold, Thermocompression									
N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R
8	0	0	0	0	0	40	27.4	5.2	12	2	14	5	7	0	0	96	28.6	6.6	22	12	49	11	1	0	0
16	0	0	2	0	0	60	27.6	9.3	18	7	26	4	5	0	0	144	30.9	6.2	30	17	81	14	2	0	0
6	0	0	1	0	0	20	26.2	6.9	4	11	3	2	0	0	0	48	30.2	4.3	9	5	33	0	1	0	0
1	0	0	0	0	0	20	28.6	6.9	3	4	10	3	0	0	0	48	31.8	4.6	12	10	26	0	0	0	0
14	0	0	0	0	0	20	30.9	4.4	8	0	11	1	0	0	0	48	30.8	4.8	15	4	21	3	4	0	0
11	0	0	0	0	1	20	30.4	5.5	6	5	9	0	0	0	0	48	30.7	5.3	9	4	32	3	0	0	0
12	0	0	0	0	0	40	30.5	4.4	10	15	12	0	1	0	0	96	32.1	5.6	25	6	62	3	0	0	0
15	0	0	0	0	0	60	29.5	5.1	27	1	25	7	0	0	0	144	30.0	5.1	30	8	101	4	1	0	0
4	0	5	0	1	6	20	30.3	5.6	0	11	8	1	0	0	0	48	31.5	4.5	3	4	39	2	0	0	0
10	0	0	0	0	0	20	33.0	3.2	10	4	6	0	0	0	0	48	30.9	5.3	13	8	25	2	0	0	0
2	1	8	1	0	4	20	28.4	5.2	4	8	6	1	1	0	0	48	32.7	4.1	8	10	27	1	2	0	0
7	0	1	0	0	0	20	32.1	4.2	7	7	6	0	0	0	0	48	32.1	5.0	11	4	28	2	3	0	0

of the first bond; N2 = Number of failures at the neck of the
lures at the second bond/wire interface; L = Number of

3

(1) Test No.	Substrate Type	Group	Chip and Substrate Attachment Method	Substrate No.	Chip-to-Substrate[1] 1 Mil Aluminum, Ultrasonic N	X̄	S	N1	N2	W	B1
202	Thick	A, B	Eutectic	3	64	5.6	1.3	35	26	0	0
	Film		Epoxy	3	64	4.9	1.1	39	17	0	1
2155	Thick	B	Eutectic	2	32	4.9	1.0	8	21	0	1
	Film		Epoxy	2	32	4.4	1.0	30	2	0	0
231	Thick	A	Eutectic	1	32	2.2	0.9	0	32	0	0
	Film			3	32	2.6	1.1	16	16	0	0
			Epoxy	1	32	2.2	1.3	10	21	0	0
				3	32	0.9	0.7	2	30	0	0
231	Thick	B	Eutectic	1	16	1.4	1.4	0	16	0	0
	Film			2	16	1.8	0.8	1	14	1	0
				3	16	0.7	0.6	0	16	0	0
			Epoxy	1	32	2.1	1.3	9	23	0	0
				2	32	1.7	1.0	3	29	0	0
				3	32	2.0	1.2	6	26	0	0
231	Thick	C	Eutectic	2	32	3.0	0.9	1	28	0	0
	Film		Epoxy	2	16	3.4	1.2	9	7	0	0

(1) 202 = As wired; 2155 = Preseal rework cycle + environmental test; 231 Group A Substrat
231 Group A Substrate 3 = Preseal rework + postseal substrate removal cycle + high temp
cycle + high temperature storage; 231 Group B Substrate 2 = Preseal rework cycle + post
seal rework cycle + high temperature storage; 231 Group C = Preseal rework cycle + pos

(2) N = Number of wire loops pulled; $\overline{X}$ = Average pull strength in grams; S = Standard deviat
at the neck of the second bond; W = Number of failures at the wire (wire broken); B1 = Nu
wire interface; L = Number of loose wires; R = Number of wire loop(s) showing bond elec

1

				Chip-to-Substrate 1 Mil Gold, Thermosonic										Substrate-to-Subst 1 Mil Aluminum, Ult					
1	B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1	B2	L	R	N	$\bar{X}$	S	N1	N2	W
0	3	0	0	64	6.3	1.6	20	35	6	1	0	0	0	40	6.2	1.0	28	11	0
1	7	0	0	64	6.5	1.8	25	11	15	1	12	0	0	40	5.1	1.3	27	7	0
1	1	0	0	16	7.3	0.9	3	10	3	0	0	0	0	20	4.4	0.9	14	4	2
0	0	0	0	32	7.5	1.1	12	14	6	0	0	0	0	20	4.2	1.4	15	5	0
0	0	0	3	32	4.4	3.2	6	9	2	14	0	0	7	20	2.4	0.7	13	7	0
0	0	0	8	32	3.3	1.7	2	24	0	0	0	0	8	20	3.8	1.7	14	5	0
0	0	0	3	32	6.4	2.0	12	13	4	3	0	0	0	20	1.6	1.2	4	16	0
0	0	0	2	32	3.9	1.7	5	24	2	1	0	0	0	20	1.4	1.0	12	8	0
0	0	0	0	16	5.2	2.1	5	7	4	0	0	0	0	10	0.7	0.7	4	6	0
0	0	0	0	16	2.1	1.9	1	15	0	0	0	0	0	10	1.3	1.2	2	8	0
0	0	0	0	16	2.2	1.2	2	14	0	0	0	0	0	10	2.1	1.0	3	6	0
0	0	1	6	32	5.7	2.0	12	17	2	0	0	0	4	20	2.0	1.2	12	8	0
0	0	0	4	32	3.9	3.1	14	15	2	1	0	0	0	20	1.3	1.0	11	7	2
0	0	0	0	32	5.9	1.4	19	9	4	0	0	0	0	20	1.6	0.7	7	13	0
0	3	0	6	32	4.9	2.5	1	15	3	13	0	1	7	20	3.4	1.0	13	6	0
0	0	0	0	16	7.7	1.1	12	1	3	0	0	0	0	10	2.8	0.9	2	8	0

strate 1 = Preseal rework cycle + postseal substrate removal cycle + high temperature storage; temperature storage; 231 Group B Substrate 1 = Preseal rework cycle + postseal rework postseal rework + high temperature storage; 231 Group B Substrate 3 = Preseal rework + post- + postseal substrate removal and repackaging + high temperature storage

eviation in grams; N1 = Number of failures at the neck of the first bond; N2 = Number of failures = Number of failures at the first bond/wire interface; B2 = Number of failures at the second bond/ electrical resistance increase

2

TABLE 16. SUMMARY OF PULL TEST
RESULTS (TEST SEQU

ubstrate Ultrasonic					Substrate-to-Substrate 2 Mil Gold, Thermocompression										Substra 2 Mil Gold, T			
W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1
0	1	0	0	0	40	25.4	7.8	3	12	14	4	7	0	0	96	26.9	6.1	23
0	1	5	0	0	40	29.9	5.3	12	9	13	3	2	0	0	96	28.1	5.3	36
2	0	0	0	0	10	31.7	2.0	0	8	0	0	0	0	0	24	27.0	5.6	3
0	0	0	0	0	20	29.3	5.6	3	5	10	0	0	0	0	48	27.7	6.7	3
0	0	0	0	7	20	31.7	3.0	3	2	15	0	0	0	0	48	29.2	4.8	6
0	0	0	0	13	20	27.8	10.9	4	4	7	5	0	0	0	48	28.8	4.8	14
0	0	0	0	0	20	31.4	5.8	5	7	6	2	0	0	0	48	26.0	5.6	14
0	0	0	0	0	20	26.2	7.3	2	5	10	3	0	0	0	48	27.9	6.8	10
0	0	0	0	0	10	31.7	2.0	5	2	3	0	0	0	0	24	25.3	9.1	7
0	0	0	0	0	10	27.8	3.4	2	0	8	0	0	0	0	24	25.4	3.1	5
0	0	0	2	0	10	29.8	5.1	4	2	0	4	0	0	0	24	29.8	5.1	7
0	0	0	0	2	20	28.8	8.5	4	4	9	3	0	0	0	48	27.0	6.3	18
2	0	0	0	5	20	28.6	4.3	4	2	14	0	0	0	0	48	28.2	3.8	16
0	0	0	0	0	20	28.8	6.1	7	8	3	2	0	0	0	48	27.1	7.0	9
0	1	0	0	9	20	30.7	5.4	1	6	12	1	0	0	0	48	28.8	5.7	6
0	0	0	0	0	10	31.8	4.8	4	0	5	1	0	0	0	24	26.1	6.3	6

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TABLE 16. SUMMARY OF PULL TEST AND ELECTRICAL TEST RESULTS (TEST SEQUENCE 2)

Substrate-to-Substrate 2 Mil Gold, Thermocompression									Substrate-to-Capacitor 2 Mil Gold, Thermocompression									
$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R
25.4	7.8	3	12	14	4	7	0	0	96	26.9	6.1	23	3	58	9	1	0	0
29.9	5.3	12	9	13	3	2	0	0	96	28.1	5.3	36	8	37	17	0	0	0
31.7	2.0	0	8	0	0	0	0	0	24	27.0	5.6	3	0	19	2	0	0	0
29.3	5.6	3	5	10	0	0	0	0	48	27.7	6.7	3	1	39	4	0	0	0
31.7	3.0	3	2	15	0	0	0	0	48	29.2	4.8	6	3	38	1	0	0	0
27.8	10.9	4	4	7	5	0	0	0	48	28.8	4.8	14	2	28	5	3	0	0
31.4	5.8	5	7	6	2	0	0	0	48	26.0	5.6	14	1	28	5	0	0	0
26.2	7.3	2	5	10	3	0	0	0	48	27.9	6.8	10	3	30	5	0	0	0
31.7	2.0	5	2	3	0	0	0	0	24	25.3	9.1	7	0	13	4	0	0	0
27.8	3.4	2	0	8	0	0	0	0	24	25.4	3.1	5	0	18	1	0	0	0
29.8	5.1	4	2	0	4	0	0	0	24	29.8	5.1	7	3	14	0	0	0	0
28.8	8.5	4	4	9	3	0	0	0	48	27.0	6.3	18	1	27	2	0	0	0
28.6	4.3	4	2	14	0	0	0	0	48	28.2	3.8	16	6	23	3	0	0	0
28.8	6.1	7	8	3	2	0	0	0	48	27.1	7.0	9	1	29	9	0	0	0
30.7	5.4	1	6	12	1	0	0	0	48	28.8	5.7	6	1	38	3	0	0	0
31.8	4.8	4	0	5	1	0	0	0	24	26.1	6.3	6	0	15	3	0	0	0

(1) Test No.	Substrate	Group	Chip and Substrate Attachment Method	Substrate No.	Chip-to-Substrate(1) 1 Mil Aluminum, Ultrasonic							
					N	$\overline{X}$	S	N1	N2	W	B1	B2
202	Thin Film	A, B	Eutectic	3	64	6.8	1.4	29	33	0	0	2
			Epoxy	3	64	5.8	1.2	49	14	0	0	1
2155	Thin Film	B	Eutectic	2	32	4.6	1.2	12	19	0	0	0
			Epoxy	2	32	4.2	1.1	32	0	0	0	0
231	Thin Film	A	Eutectic	1	32	3.6	0.8	6	25	0	0	0
				3	32	3.2	1.1	0	32	0	0	0
			Epoxy	1	32	2.3	1.3	14	12	6	0	0
				3	32	3.0	1.7	16	16	0	0	0
231	Thin Film	B	Eutectic	1	16	1.9	1.3	5	11	0	0	0
				2	16	1.9	0.8	1	15	0	0	0
				3	16	2.6	1.4	0	16	0	0	0
	Thin Film		Epoxy	1	32	2.8	1.2	18	13	0	0	0
				2	32	2.6	1.0	9	22	1	0	0
				3	16	3.2	1.4	3	13	0	0	0
231	Thin Film	C	Eutectic	2	32	3.5	1.5	12	9	7	0	3
			Epoxy	2	32	3.8	1.0	19	13	0	0	0

(1) 202 = As wired; 2155 = Preseal rework cycle + environmental test; 231 Group A Substrate 1
231 Group A Substrate 3 = Preseal rework + postseal substrate removal cycle + high temper
cycle + high temperature storage; 231 Group B Substrate 2 = Preseal rework cycle + postse
seal rework cycle + high temperature storage; 231 Group C = Preseal rework cycle + posts

(2) N = Number of wire loops pulled; $\overline{X}$ = Average Pull strength in grams; S = Standard deviatio
ures at the neck of the second bond; W = Number of failures at the wire (wire broken); B1 =
second bond/wire interface; L = Number of loose wires; R = Number of wire loop(s) showin

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R	Chip-to-Substrate 1 Mil Gold, Thermosonic										Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic						
	N	$\bar{X}$	S	N1	N2	W	B1	B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1
;	64	6.8	1.3	22	29	10	0	2	0	0	40	7.1	1.4	14	26	0	0
)	64	7.2	0.9	30	18	15	1	0	0	0	40	7.4	1.2	28	12	0	0
)	32	6.5	1.4	12	18	1	0	0	0	0	20	5.0	1.0	10	10	0	0
)	32	6.8	2.0	13	15	4	0	0	0	0	20	3.9	2.0	8	11	0	0
)	32	6.3	1.8	11	16	3	0	0	0	0	20	3.4	1.0	9	11	0	0
)	32	3.9	2.0	2	28	2	0	0	0	0	20	3.5	1.0	11	9	0	0
)	32	6.8	1.2	20	6	6	0	0	0	0	20	3.5	1.0	11	9	1	0
)	32	5.9	1.1	20	6	6	0	0	0	0	20	3.6	1.7	14	5	1	0
)	16	6.6	0.8	7	1	8	0	0	0	0	10	1.3	1.0	2	8	0	0
)	16	2.0	1.7	2	13	0	1	0	0	0	10	2.2	0.8	4	6	0	0
D	16	2.6	1.7	0	16	0	0	0	0	0	10	4.6	0.8	8	1	1	0
)	32	6.4	1.7	20	8	2	0	0	0	0	20	3.5	0.9	15	3	2	0
D	32	3.4	2.4	3	20	0	9	0	0	1	20	2.2	0.9	14	5	1	0
D	16	6.0	1.3	4	11	1	0	0	0	0	10	4.8	1.3	6	3	1	0
2	30	4.1	2.1	0	10	1	18	0	2	9	20	2.4	1.3	10	9	0	0
)	32	7.3	1.4	15	7	10	0	0	0	0	20	4.4	1.1	11	8	1	0

eal rework cycle + postseal substrate removal cycle + high temperature storage;
:orage; 231 Group B Substrate 1 = Preseal rework cycle + postseal rework
:k + high temperature storage; 231 Group B Substrate 3 = Preseal rework + post-
trate removal and repackaging + high temperature storage

ms; N1 = Number of failures at the neck of the first bond; N2 = Number of fail-
of failures at the first bond/wire interface; B2 = Number of failures at the
ectrical resistance increase

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TABLE 17. SUMMARY OF PULL TEST AND
RESULTS (TEST SEQUENC

...trate ...trasonic				Substrate-to-Substrate 2 Mil Gold, Thermocompression										Substrate-to... 2 Mil Gold, Ther...				
B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2
0	0	0	0	40	25.7	8.9	6	10	11	4	9	0	0	96	27.9	4.3	30	7
0	0	0	0	40	31.4	7.6	18	3	13	6	0	0	0	96	29.7	4.7	39	18
0	0	0	0	20	29.1	5.4	2	5	11	2	0	0	0	48	28.1	4.7	6	0
0	0	0	0	20	33.2	2.7	1	5	18	0	0	0	0	48	29.0	5.5	15	0
0	0	0	0	20	29.7	4.8	5	7	8	0	0	0	0	48	29.0	5.0	8	1
0	0	0	0	20	23.8	10.9	4	3	6	6	1	0	0	48	29.5	3.9	9	3
0	0	0	0	20	29.6	9.0	7	5	5	3	0	0	0	48	26.0	8.8	18	3
0	0	0	0	20	29.5	5.9	2	5	11	2	0	0	0	48	28.0	4.9	11	3
0	0	0	0	10	33.0	1.6	0	3	7	0	0	0	0	24	28.0	3.7	5	0
0	0	0	0	10	29.3	5.1	1	3	6	0	0	0	0	24	28.0	4.4	6	0
0	0	0	0	10	29.3	3.2	4	4	2	0	0	0	0	24	28.5	5.8	4	1
0	0	0	0	20	32.8	4.0	4	3	13	0	0	0	0	48	27.5	5.5	12	2
0	0	0	1	20	29.6	3.6	3	5	12	0	0	0	0	48	25.3	5.8	17	1
0	0	0	0	10	31.5	3.6	2	3	4	1	0	0	0	24	28.5	3.6	6	0
0	0	1	9	20	32.5	3.4	0	9	11	0	0	0	0	48	29.3	5.2	6	5
0	0	0	3	20	30.1	7.8	1	5	11	3	0	0	0	48	28.7	5.0	13	3

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TABLE 17. SUMMARY OF PULL TEST AND ELECTRICAL TEST RESULTS (TEST SEQUENCE 2)

Substrate-to-Substrate 2 Mil Gold, Thermocompression									Substrate-to-Capacitor 2 Mil Gold, Thermocompression									
$\overline{X}$	S	N1	N2	W	B1	B2	L	R	N	$\overline{X}$	S	N1	N2	W	B1	B2	L	R
25.7	8.9	6	10	11	4	9	0	0	96	27.9	4.3	30	7	55	4	0	0	0
31.4	7.6	18	3	13	6	0	0	0	96	29.7	4.7	39	18	28	5	1	0	0
29.1	5.4	2	5	11	2	0	0	0	48	28.1	4.7	6	0	40	2	0	0	0
33.2	2.7	1	5	18	0	0	0	0	48	29.0	5.5	15	0	31	2	0	0	0
29.7	4.8	5	7	8	0	0	0	0	48	29.0	5.0	8	1	35	3	1	0	0
23.8	10.9	4	3	6	6	1	0	0	48	29.5	3.9	9	3	31	4	1	0	0
29.6	9.0	7	5	5	3	0	0	0	48	26.0	8.8	18	3	17	9	1	0	0
29.5	5.9	2	5	11	2	0	0	0	48	28.0	4.9	11	3	31	3	0	0	0
33.0	1.6	0	3	7	0	0	0	0	24	28.0	3.7	5	0	19	0	0	0	0
29.3	5.1	1	3	6	0	0	0	0	24	28.0	4.4	6	0	17	1	0	0	0
29.3	3.2	4	4	2	0	0	0	0	24	28.5	5.8	4	1	17	2	0	0	0
32.8	4.0	4	3	13	0	0	0	0	48	27.5	5.5	12	2	29	4	1	0	0
29.6	3.6	3	5	12	0	0	0	0	48	25.3	5.8	17	1	25	1	0	0	1
31.5	3.6	2	3	4	1	0	0	0	24	28.5	3.6	6	0	18	0	0	0	0
32.5	3.4	0	9	11	0	0	0	0	48	29.3	5.2	6	5	36	1	0	0	0
30.1	7.8	1	5	11	3	0	0	0	48	28.7	5.0	13	3	27	4	1	0	0

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(1) Test No.	Substrate Type	Group	Chip and Substrate Attachment Method	Substrate No.	Chip-to-Substrate(2) 1 Mil Aluminum, Ultrasonic							
					N	$\overline{X}$	S	N1	N2	W	B1	B2
302	Thick Film	A, B	Epoxy	3	64	7.0	0.8	20	43	0	0	1
314	Thick Film	A, B	Epoxy	2	64	4.4	1.0	28	36	0	0	0
				3	64	4.0	1.0	9	53	0	0	0
326	Thick Film	A, B	Epoxy	2	64	4.5	1.3	39	25	0	0	0
				3	64	4.7	1.2	32	32	0	0	0
338	Thick Film	A	Epoxy	1	32	2.8	1.0	14	18	0	0	0
				2	32	2.7	1.1	5	27	0	0	0
				3	32	2.7	1.2	7	25	0	0	0
342	Thick Film	B	Epoxy	1	32	3.5	1.3	1	31	0	0	0
				2	32	2.3	1.3	4	28	0	0	0
				3	32	3.0	1.6	8	24	0	0	0
302	Thin Film	A, B	Epoxy	3	64	6.7	1.3	50	14	0	0	0
314	Thin Film	A, B	Epoxy	2	64	5.0	1.1	47	17	0	0	0
				3	64	5.2	1.1	33	31	0	0	0
326	Thin Film	A, B	Epoxy	2	64	5.2	1.2	59	4	0	1	0
				3	64	4.7	1.3	63	1	0	0	0
338	Thin Film	A	Epoxy	1	32	4.0	1.3	12	20	0	0	0
				2	32	4.5	1.5	11	21	0	0	0
				3	32	4.6	1.3	19	13	0	0	0
342	Thin Film	B	Epoxy	1	32	3.7	0.9	17	14	1	0	0
				2	32	2.0	1.1	13	19	0	0	0
				3	32	2.8	1.0	17	15	1	0	0

(1) 302 = As wired; 314 Substrate 2 = Preseal rework cycle; 314 Substrate 3 = Preseal rewor rework + postseal rework; 338 Substrate 1 = Preseal rework cycle + two postseal rework c 3 = Preseal rework and two postseal reworks; 342 Substrate 1 = Preseal rework cycle + tw cycle + two postseal reworks + high temperature storage; 342 Substrate 3 = Preseal rewor

(2) N = Number of wire loops pulled; $\overline{X}$ = Average pull strength in grams; S = Standard deviati ures at the neck of the second bond; W = Number of failures at the wire (wire broken); B1 second bond/wire interface; L = Number of loose wires; R = Number of wire loop(s) showi

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			Chip-to-Substrate 1 Mil Gold, Thermosonic										Substrate-to-Substrat 1 Mil Aluminum, Ultras						
B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1	B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1
1	0	0	64	7.1	1.1	35	19	10	0	0	0	0	40	7.2	1.3	29	9	0	0
0	0	0	64	7.2	1.5	34	19	11	0	0	0	0	40	5.3	0.9	22	18	0	0
0	0	0	64	6.1	2.0	23	35	4	0	0	0	0	40	4.7	1.0	25	15	0	0
0	0	0	64	4.9	1.8	15	1	0	0	0	0	0	40	5.4	0.1	32	8	0	0
0	0	0	64	5.1	1.9	18	43	3	0	0	0	0	40	5.1	1.4	27	13	0	0
0	0	0	32	7.6	1.3	16	6	10	0	0	0	0	20	3.5	1.5	14	6	0	0
0	0	0	32	5.7	2.2	5	18	7	2	0	0	0	20	2.7	0.8	11	9	0	0
0	0	0	32	5.0	1.8	7	21	3	1	0	0	0	20	2.7	0.7	5	15	0	0
0	0	4	32	7.3	1.5	14	9	8	1	0	0	0	20	3.2	1.2	7	5	0	0
0	0	7	32	4.2	2.4	5	15	0	12	0	0	14	20	2.3	1.1	16	3	0	5
0	0	6	32	4.9	2.1	11	17	0	3	0	0	3	20	2.5	1.0	11	9	0	1
0	0	0	64	7.4	1.1	34	10	20	0	0	0	0	40	7.5	1.5	33	7	0	0
0	0	0	64	7.3	1.4	38	17	9	0	0	0	0	40	5.8	0.7	38	2	0	0
0	0	0	64	6.1	1.4	31	30	3	0	0	0	0	40	5.2	0.8	36	4	0	0
0	0	0	64	5.8	1.5	25	31	5	0	3	0	0	40	5.9	1.7	33	6	1	0
0	0	0	64	5.8	1.2	23	40	1	0	0	0	0	40	5.6	1.2	31	9	0	0
0	0	0	32	7.1	1.2	14	10	8	0	0	0	0	20	5.3	1.2	12	8	0	0
0	0	0	32	5.5	1.6	9	20	2	1	0	0	0	20	3.1	1.1	8	12	0	0
0	0	0	32	5.8	1.8	11	20	1	0	0	0	0	20	4.4	1.9	13	7	0	0
0	0	0	32	7.4	1.1	15	10	7	0	0	0	0	20	4.1	1.1	14	5	0	0
0	0	0	32	3.8	2.2	2	12	2	15	0	0	3	20	3.1	0.9	8	12	0	0
0	0	0	32	4.8	2.7	7	10	1	14	0	0	6	20	3.4	0.7	10	10	0	0

rk; 326 Substrate 2 = Preseal rework cycle + postseal rework; 326 Substrate 3 = Preseal
cycles; 338 Substrate 2 = Preseal rework cycle + two postseal reworks; 338 Substrate
two postseal rework cycles + high temperature storage; 342 Substrate 2 = Preseal rework
rk + two postseal reworks + high temperature storage

tion in grams; N1 = Number of failures at the neck of the first bond; N2 = Number of fail-
= Number of failures at the first bond/wire interface; B2 = Number of failures at the
ing bond electrical resistance increase

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TABLE 18. SUMMARY OF PULL TEST AND ELEC
(TEST SEQUENCE 3)

ate asonic				Substrate-to-Substrate 2 Mil Gold, Thermocompression										Substrate-to-Ca 2 Mil Gold, Thermo				
B1	B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1	B2	L	R	N	$\bar{X}$	S	N1	N2
0	0	0	0	40	32.2	4.0	7	17	16	0	0	0	0	96	26.7	7.8	30	5
0	0	0	0	40	31.8	3.0	6	15	18	1	0	0	0	96	28.6	6.6	16	3
0	0	0	0	40	26.6	8.2	3	11	11	6	9	0	0	96	29.1	5.4	21	2
0	0	0	0	40	28.4	6.0	14	9	13	4	0	0	0	96	29.4	5.5	37	5
0	0	0	0	40	29.0	6.2	7	9	21	3	0	0	0	96	28.9	6.4	19	8
0	0	0	0	20	33.8	2.6	0	9	11	0	0	0	0	48	29.9	5.3	9	1
0	0	0	0	20	32.7	4.3	3	0	16	1	0	0	0	48	30.2	5.0	3	1
0	0	0	0	20	29.8	7.2	2	1	16	1	0	0	0	48	30.6	4.1	6	2
0	1	0	9	20	32.7	1.8	2	2	16	0	0	0	0	48	28.5	6.7	7	4
5	0	0	10	20	31.0	5.6	2	4	14	0	0	0	0	48	30.4	4.3	13	1
1	0	0	2	20	32.9	3.0	3	0	16	0	0	0	0	48	29.9	4.0	15	2
0	0	0	0	40	33.1	4.1	26	1	12	1	0	0	0	96	28.5	5.8	42	3
0	0	0	0	40	33.7	5.2	8	3	27	0	2	0	0	96	28.2	4.7	13	2
0	0	0	0	40	30.1	5.2	12	9	17	2	1	0	0	96	29.1	4.5	21	3
0	0	0	0	40	28.6	5.2	12	9	12	7	0	0	0	96	31.2	5.2	19	6
0	0	0	0	40	27.9	1.7	11	5	20	4	0	0	0	96	30.9	6.0	29	9
0	0	0	0	20	34.6	2.6	0	4	16	0	0	0	0	48	27.7	7.2	3	1
0	0	0	0	20	29.9	5.7	7	2	10	1	0	0	0	48	28.8	4.2	14	2
0	0	0	0	20	29.6	4.2	2	0	17	1	0	0	0	48	28.7	5.7	13	2
0	0	0	0	20	32.7	4.4	4	1	14	1	0	0	0	48	28.4	5.4	8	1
0	0	0	3	20	31.4	3.0	8	0	12	0	0	0	0	48	29.6	3.8	16	0
0	0	0	0	20	31.0	3.5	5	1	14	0	0	0	0	48	29.5	5.2	20	1

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TABLE 18. SUMMARY OF PULL TEST AND ELECTRICAL TEST RESULTS, (TEST SEQUENCE 3)

Substrate-to-Substrate 2 Mil Gold, Thermocompression									Substrate-to-Capacitor 2 Mil Gold, Thermocompression									
$\bar{X}$	S	N1	N2	W	B1	B2	L	R	N	$\bar{X}$	S	N1	N2	W	B1	B2	L	R
32.2	4.0	7	17	16	0	0	0	0	96	26.7	7.8	30	5	44	17	1	0	0
31.8	3.0	6	15	18	1	0	0	0	96	28.6	6.6	16	3	63	12	0	0	0
26.6	8.2	3	11	11	6	9	0	0	96	29.1	5.4	21	2	65	7	0	0	0
28.4	6.0	14	9	13	4	0	0	0	96	29.4	5.5	37	5	48	5	1	0	0
29.0	6.2	7	9	21	3	0	0	0	96	28.9	6.4	19	8	57	8	2	0	0
33.8	2.6	0	9	11	0	0	0	0	48	29.9	5.3	9	1	31	6	1	0	0
32.7	4.3	3	0	16	1	0	0	0	48	30.2	5.0	3	1	42	1	1	0	0
29.8	7.2	2	1	16	1	0	0	0	48	30.6	4.1	6	2	38	1	1	0	0
32.7	1.8	2	2	16	0	0	0	0	48	28.5	6.7	7	4	33	3	1	0	0
31.0	5.6	2	4	14	0	0	0	0	48	30.4	4.3	13	1	32	0	2	0	0
32.9	3.0	3	0	16	0	0	0	0	48	29.9	4.0	15	2	28	0	3	0	0
33.1	4.1	26	1	12	1	0	0	0	96	28.5	5.8	42	3	47	4	0	0	0
33.7	5.2	8	3	27	0	2	0	0	96	28.2	4.7	13	2	78	3	0	0	0
30.1	5.2	12	9	17	2	1	0	0	96	29.1	4.5	21	3	67	5	0	0	0
28.6	5.2	12	9	12	7	0	0	0	96	31.2	5.2	19	6	65	5	0	0	0
27.9	1.7	11	5	20	4	0	0	0	96	30.9	6.0	29	9	50	8	0	0	0
34.6	2.6	0	4	16	0	0	0	0	48	27.7	7.2	3	1	39	5	0	0	0
29.9	5.7	7	2	10	1	0	0	0	48	28.8	4.2	14	2	32	0	0	0	0
29.6	4.2	2	0	17	1	0	0	0	48	28.7	5.7	13	2	31	1	0	0	0
32.7	4.4	4	1	14	1	0	0	0	48	28.4	5.4	8	1	38	1	0	0	0
31.4	3.0	8	0	12	0	0	0	0	48	29.6	3.8	16	0	29	0	3	0	0
31.0	3.5	5	1	14	0	0	0	0	48	29.5	5.2	20	1	24	0	3	0	0

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9.2.1 Interpretation of control specimen results (test sequence No. 1).

(a) Ultrasonic Aluminum Interconnections. The average pull strength of as-wired ultrasonic aluminum bonds was generally lower on eutectically attached specimens than on those attached with epoxy. This is probably due to flux contamination being present on the gold substrate conductors during the chip attachment process. The $S/\overline{X}$ ratio* for aluminum wires is greater on eutectically bonded specimens. The pull strength is greater on thin film than on thick film substrates.

The pull strength of ultrasonic aluminum bonds tended to decrease, by 30 to 50 percent, and the $S/\overline{X}$ ratio increased after environmental tests and after high temperature storage (150°C/1000 hours). Lowering of the tensile strength of the aluminum wire upon annealing, as indicated from the data of Table 19, is the primary cause of the degradation. The predominant failure modes were at the neck of either first or second bonds (N1 or N2), which is a part of the wire.

A total of 11 wire bonds indicated bond electrical resistance increases after environmental tests and 10 bonds showed resistance increases after high temperature storage (150°C). Almost all such increases were on the eutectically attached specimens. Visually, these substrates were not as clean as epoxy bonded specimens. Failure mode data indicates that these bonds are more likely to fail, at a lower load, at the bimetallic interface; i.e., B2 for chip-to-substrate and B1 or B2 for substrate-to-substrate. The two loose wires detected during the tests were all on substrates exhibiting a large number of resistance increases. It is theorized that the incomplete removal of flux may have accelerated the aluminum/gold interface diffusion, resulting in a weaker joint.

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*The ratio S/X = standard deviation of the bond pull strength (grams)/mean of the bond pull strength (grams), as determined by the destructive wire bond pull test. The significance of this ratio is explained in Appendix A.

TABLE 19. TENSILE STRENGTH DEGRADATION OF 0.001 INCH GOLD AND ALUMINUM WIRE AS A FUNCTION OF ANNEALING CONDITIONS

Wire Treatment (in air)	Tensile strength of 0.001 inch diameter gold wire (grams of force)*	Tensile strength of 0.001 inch diameter aluminum wire (grams of force)*
Not annealed	6.6	16.2
$125^{\circ}C$, 2 hours	—	12.0
$125^{\circ}C$, 20 hours	—	10.6
$125^{\circ}C$, 200 hours	—	8.7
$125^{\circ}C$, 500 hours	—	8.1
$150^{\circ}C$, 2 hours	6.6	10.7
$150^{\circ}C$, 20 hours	6.4	8.8
$150^{\circ}C$, 200 hours	6.3	7.1
$150^{\circ}C$, 1000 hours	6.0	6.4

*Wire clamped at both ends, pulled using an Instron tensile strength tester, at a rate of 0.5 inch/minute.

(b) Thermosonic Gold Interconnection. The pull strength and $S/\overline{X}$ ratio of as-wired thermosonic chip-to-substrate bonds were superior to those of the ultrasonic aluminum chip-to-substrate bonds. The thermosonic bonds were not degraded after environmental tests and high temperature storage. This is to be expected since the tensile strength of gold wire remains essentially unchanged after thermal aging (see Table 19).

Flux contamination of chips or gold conductors could result in a lower pull strength, a higher $S/\overline{X}$ ratio and a wire bond electrical resistance increase on eutectically attached substrates, after environmental tests and high temperature storage. Examples are one eutectically bonded substrate in test number 113 and test number 117 which had average pull strengths of 2.3 and 2.0 grams with $S/\overline{X}$ ratios in excess of 90 percent.

The predominant failure modes for thermosonic gold bonding were fractures at the neck of the first or second bond or the fracture of the wire itself (N1, N2 and W). There were no loose wires detected.

(c) Thermocompression Gold Interconnections. The quality of pulse thermocompression gold wire bonds showed that this was the most reliable interconnection among those studied. The average pull strength of 2 mil diameter wire was greater than 20 gms with a $S/\overline{X}$ less than 20 percent. The bonds were not degraded during environmental testing and high temperature storage (150°C).

9.2.2 Effect of preseal rework. Table 20 summarizes the pull test data of preseal reworked interconnections on epoxy attached specimens. It can be seen that: (1) the reworked interconnections (test number 314, substrate number 3) were as good as the control (test number 113) after the environmental tests, (2) the reliability of the interconnections on the neighboring substrate (test number 314, substrate number 2) was not influenced by the preseal rework. This applies to all interconnection types, all substrate types and all package types. There were no loose wires or detectable bond electrical resistance increases.

The results presented in Table 21 indicate that the preseal rework of eutectically attached devices and substrates does not affect the interconnection reliability on the neighboring substrates (test number 2155).

9.2.3 Effect of postseal rework. The reliability of interconnections, both reworked and on the neighboring substrates, is not affected by the postseal rework of epoxy attached devices and substrates, as it is seen from Table 22. This applies to all interconnection types, substrate types and package types. There were no loose wires or increases in bond electrical resistance. Decreased interconnection reliability may result, however, if the package delidding operation is not done properly, due to handling or attaching of wire bonds by molten solder.

TABLE 20. EFFECT OF PRESEAL INTERCONNECTION REWORK ON EPOXY ATTACHED SUBSTRATES

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 1 Mil Gold, Thermocompression		Substrate-to-Capacitor 1 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 113)	3.6	1.7	6.1	1.9	4.2	1.3	28.6	6.1	31.8	4.6
	Preseal rework cycle - Test No. 314 Subst. 2	4.4	1.0	7.2	1.5	5.3	0.9	31.8	3.0	28.6	6.6
	Preseal reworked - Test No. 314 Subst. 3	4.0	1.0	6.1	2.0	4.7	1.0	26.6	8.2	29.1	5.4
Thin Film	Control (Test No. 113)	4.9	0.9	7.7	0.8	4.0	1.6	33.0	3.2	30.9	5.3
	Preseal rework cycle - Test No. 314 Subst. 2	5.0	1.1	7.3	1.4	5.8	0.7	33.7	5.2	28.2	4.7
	Preseal reworked - Test No. 314 Subst. 3	5.2	1.1	6.1	1.4	5.2	0.8	30.1	5.2	29.1	4.5

TABLE 21. EFFECT OF PRESEAL INTERCONNECTION REWORK ON EUTECTIC ATTACHED SUBSTRATES

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 2 Mil Gold, Thermocompression		Substrate-to-Capacitor 2 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 113)	3.6	1.0	4.3	3.0	3.6	1.0	26.3	6.9	30.2	4.3
	Preseal rework cycle - Test No. 2155	4.7	1.1	7.5	1.0	4.4	0.9	30.6	4.7	27.4	6.3
Thin Film	Control (Test No. 113)	2.4	1.5	5.7	1.8	3.2	2.0	30.3	5.6	31.5	4.5
	Preseal rework cycle - Test No. 2155	4.4	1.0	6.6	1.7	4.4	1.6	31.2	4.9	28.5	5.2

TABLE 22. EFFECT OF POSTSEAL REWORK INTERCONNECTIONS ON EPOXY ATTACHED SUBSTRATES

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 2 Mil Gold, Thermocompression		Substrate-to-Capacitor 2 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 113)	3.6	1.7	6.1	1.9	4.2	1.3	28.6	6.1	31.8	4.6
	Postseal reworked - Test No. 326 Subst. 2	4.5	1.3	4.9	1.8	5.4	1.0	28.4	6.0	29.4	5.5
	Postseal reworked - Test No. 326 Subst. 3	4.7	1.2	5.1	1.9	5.1	1.4	29.0	6.2	28.9	6.4
Thin Film	Control (Test No. 113)	4.9	0.9	7.7	0.8	4.0	1.6	33.0	3.2	30.9	5.3
	Postseal reworked - Test No. 326 Subst. 2	5.2	1.2	5.8	1.5	5.9	1.7	28.6	5.2	31.2	5.2
	Postseal reworked - Test No. 326 Subst. 3	4.7	1.3	5.8	1.2	5.6	1.2	27.9	1.7	30.9	6.0

For interconnections on eutectically attached devices or substrates, the reworked ultrasonic aluminum and thermosonic gold wire bonds (substrate number 2) were inferior to those on the non-reworked control specimens fabricated from both thick and thin film substrates. These results are summarized in Table 23. One loose wire and a few bond electrical resistance increases were detected. Although the quantity of specimens was limited, and the high temperature storage test (150°C) employed was substantially more severe than normally required, it can be said that reworked interconnections involving bimetallic interfaces are less reliable. Causes of degradation are increased flux contamination and high device rework process temperatures. The reliability of reworked thermocompression gold bonds, which interconnects gold wire to either gold or silver-palladium metallization, is not affected.

Rework of eutectically attached devices tended to degrade the reliability of ultrasonic aluminum interconnections on the neighboring substrate. Thermosonic gold wire bonds were less affected. For pulsed thermocompression gold bonding, there was no effect.

9.2.4 Effect of multiple reworks. The multiple interconnection rework performed was restricted to devices and substrates that were epoxy attached. Results presented in Table 24 indicate that, after the environmental tests, the reworked interconnections are comparable to those of the control specimens. There were no loose wires or increases in bond electrical resistance, as seen from Table 18. Slightly lower pull strengths on some of the reworked ultrasonic aluminum and thermosonic gold wire bonds are probably due to the increased contaminations on the gold conductors. Multiple interconnection rework had no significant effect on the reliability of the interconnections on the neighboring substrates.

After high temperature storage (150°C), the pull strength of reworked ultrasonic aluminum thermosonic gold interconnections appears to be slightly inferior to those of the control specimens, probably due to the aforementioned causes. There were no loose wires. Some bond electrical resistance increases were found on interconnections involving bimetallic interfaces. It should be emphasized, however, that high temperature

TABLE 23. EFFECT OF POSTSEAL INTERCONNECTION REWORK ON EUTECTIC ATTACHED SUBSTRATES

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 2 Mil Gold, Thermocompression		Substrate-to-Capacitor 2 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 117)	2.4	0.9	4.2	2.9	2.9	0.9	30.9	4.4	30.8	4.8
	Postseal rework cycle - Test No. 231 Group B Substrate 1	1.4	1.4	5.2	2.1	0.7	0.7	31.7	2.0	25.3	9.1
	Postseal reworked - Test No. 231 Group B Substrate 2	1.8	0.8	2.1	1.9	1.3	1.2	27.8	3.4	25.4	3.1
Thin Film	Control (Test No. 117)	3.9	1.7	7.0	1.5	3.9	1.9	28.4	5.2	32.7	4.1
	Postseal rework cycle - Test No. 231 Group B Substrate 1	1.9	1.3	6.6	0.8	1.3	1.0	33.0	1.6	28.0	3.7
	Postseal reworked - Test No. 231 Group B Substrate 2	1.9	0.8	2.0	1.7	2.2	0.8	29.3	5.1	28.0	4.4

TABLE 24. EFFECT OF MULTIPLE INTERCONNECTION REWORKS ON EPOXY ATTACHED SUBSTRATE AFTER ENVIRONMENTAL TEST

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 2 Mil Gold, Thermocompression		Substrate-to-Capacitor 2 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 113)	3.6	1.7	6.1	1.9	4.2	1.3	28.6	6.1	31.8	4.6
	1 Preseal and 2 Post-seal rework cycles (Test No. 338 Subst. 1)	2.8	1.0	7.6	1.3	3.5	1.5	33.8	2.6	29.9	5.3
	2 Postseal reworks (Test No. 338 Subst. 2)	2.7	1.1	5.7	2.2	2.7	0.8	32.7	4.3	30.2	5.0
	1 Preseal and 2 Post-seal reworks (Test No. 338 Subst. 3)	2.7	1.2	5.0	1.8	2.7	0.7	29.8	7.2	30.6	4.1
Thin Film	Control (Test No. 113)	4.9	0.9	7.7	0.8	4.0	1.6	33.0	3.2	30.9	5.3
	1 Preseal and 2 Post-seal rework cycles (Test No. 338 Subst. 1)	4.0	1.3	7.1	1.2	5.3	1.2	34.7	2.6	27.7	7.2
	2 Postseal reworks (Test No. 338 Subst. 2)	4.5	1.5	5.5	1.6	3.1	1.1	29.9	5.7	28.8	4.2
	1 Preseal and 2 Post-seal reworks (Test No. 338 Subst. 3)	4.6	1.3	5.8	1.8	4.4	1.9	29.6	4.2	28.7	5.7

storage tests (150°C) performed in this program were very severe and is not required in most hybrid screening tests. These results are summarized in Table 25.

9.3 Significance of results.

- The bond strength of reworked thermocompression gold wire interconnections, both from substrate-to-substrate and from substrate-to-capacitor, were as good as those of the initial bonds. This applies to all substrate types, all device and substrate attachment methods and all package types. The pull strength does not degrade as a result of environmental tests or high temperature storage. Multiple interconnection rework has no effect on the reliability of TC gold wire bonds already on the circuit.

- Reworked ultrasonic aluminum interconnections, both from chip-to-substrate and from substrate-to-substrate, on epoxy attached devices or substrates, are as reliable as the non-reworked. The pull strength is generally better on thin film substrates than on thick film substrates. Multiple rework has no effect on the reliability of the aluminum wire bonds already on the hybrid circuit. Under severe accelerated test conditions, such as high temperature storage (150°C/1000 hours), bond electrical resistance may increase, possibly due to gold-aluminum intermetallic compound formation and the growth of Kirkendall voids.

- Reworked thermosonic gold interconnections, from chip-to-substrate, on epoxy attached devices or substrates, are as reliable as non-reworked thermosonic gold bonds. The pull strength is generally better than for ultrasonic aluminum bonding. Multiple rework has no effect on the reliability of the wire bonds already on the hybrid circuit. Bond electrical resistance may increase following high temperature storage tests (150°C).

TABLE 25. EFFECT OF MULTIPLE INTERCONNECTION REWORKS ON EPOXY ATTACHED SUBSTRATE AFTER HIGH TEMPERATURE STORAGE

		Chip-to-Substrate 1 Mil Aluminum, Ultrasonic		Chip-to-Substrate 1 Mil Gold, Thermosonic		Substrate-to-Substrate 1 Mil Aluminum, Ultrasonic		Substrate-to-Substrate 2 Mil Gold, Thermocompression		Substrate-to-Capacitor 2 Mil Gold, Thermocompression	
		$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)	$\overline{X}$ (gms)	S (gms)
Thick Film	Control (Test No. 117)	3.4	1.2	6.9	1.2	3.1	1.2	30.4	5.5	30.7	5.3
	1 Preseal and 2 Postseal rework cycles (Test No. 342 Subst. 1)	3.5	1.3	7.3	1.5	3.2	1.2	32.7	1.8	28.5	6.7
	2 Postseal reworks (Test No. 342 Subst. 2)	2.3	1.3	4.2	2.4	2.3	1.1	31.0	5.6	30.9	4.3
	1 Preseal and 2 Postseal reworks (Test No. 342 Subst. 3)	3.0	1.6	4.9	2.1	2.5	1.0	32.9	3.0	29.9	4.0
Thin Film	Control (Test No. 117)	4.2	0.9	7.5	0.8	3.9	1.9	32.1	4.2	32.1	5.0
	1 Preseal and 2 Postseal rework cycles (Test No. 342 Subst. 1)	3.7	0.9	7.4	1.1	4.1	1.1	32.7	4.4	28.4	5.4
	2 Postseal reworks (Test No. 342 Subst. 2)	2.0	1.1	3.8	2.2	3.1	0.9	31.4	3.0	29.6	3.8
	1 Preseal and 2 Postseal reworks (Test No. 342 Subst. 3)	2.8	1.0	4.8	2.7	3.4	0.7	31.0	3.5	29.5	5.2

- Reworked ultrasonic aluminum and thermosonic gold interconnections on eutectically attached devices or substrates are inferior to their non-reworked counterparts. This applies to all substrate types or package types used in this program. The high temperatures employed during the device attachment rework process and flux contamination are responsible for the degradation of bond quality, both mechanically and electrically.

10.0 TASK V. PACKAGE REPLACEMENT

10.1 Objectives. The objective of the package replacement evaluation was to determine the effects of substrate removal and repackaging by thermal means on hybrid-component reliability.

Substrates attached using eutectic alloys were of particular interest because over-heating of the substrates and various circuit elements could occur during substrate removal.

10.2 Results. Removal of substrates from old packages and remounting into new packages was not difficult technically, whether the substrate was bonded to the package by epoxy or by gold/tin eutectic. The quality of substrate-to-package bonds in repackaged hybrids was as good as that of the bonds in the original package. Leaching of the gold or platinum/gold conductor had no significant effect on the melting point or fluidity of the eutectic. Repackaging of eutectically attached substrates had little effect on device-to-substrate epoxy bonds.

The pull test data summarized in Table 26 suggests that the reliability of interconnections on epoxy attached substrates, (as determined after high temperature storage), was not affected by replacement of the package, after high temperature storage.

For eutectically attached substrates, the reliability of thermocompression gold bonds was not affected by the replacement of packages. Interconnections involving bimetallic interfaces, however, appear to be less reliable than the control specimens since the repackaged hybrids had a greater number of bonds exhibiting an increase of electrical resistance (42 as compared with 18 for the controls) and loose wires (4 as compared with none for the controls) after high temperature storage. It should be pointed out that there was only one loose wire and no bond resistance increases following the environmental tests.

10.3 Significance of results.

- The reliability of the test specimen hybrids was not affected by the replacement of packages in which the substrates are attached by epoxy. This applies to all five types of interconnections

TABLE 26. SUMMARY OF TEST RESULTS FOR PACKAGE REPLACEMENT

	Substrate Attachment Method	Substrate Type	Leak Test (1)	PIN Test (2)	Pull Test Results (3): Chip-to-Substrate, 1 Mil Aluminum, Ultrasonic			Chip-to-Substrate, 1 Mil Gold, Thermosonic			Substrate-to-Substrate, 1 Mil Aluminum, Ultrasonic			Substrate-to-Substrate 2 Mil Gold, Thermocompression			Substrate-to-Substrate, 2 Mil Gold Thermocompression		
					$\bar{X}$	S	R	$\bar{X}$	S	R	$\bar{X}$	S	R	$\bar{X}$	S	R	$\bar{X}$	S	R
Control (Test No. 117)	Eutectic	Thick Film	2/2	2/2	2.4	0.9	0	4.2	2.9	8	2.9	0.9	0	30.9	4.4	0	30.8	4.8	0
		Thin Film	2/2	2/2	3.9	1.7	5	7.0	1.5	1	3.9	1.9	4	28.4	5.2	0	32.7	4.1	0
Substrates Repackaged (Test No. 231, Group C)	Eutectic	Thick Film	2/2	2/2	3.0	0.9	6	4.9	2.5	7	3.4	1.0	9	30.7	5.4	0	28.8	5.7	0
		Thin Film	2/2	2/2	3.5	1.5	2	4.1	2.1	9	2.4	1.3	9	32.5	3.4	0	29.3	5.2	0
Control (Test No. 117)	Epoxy	Thick Film	2/2	2/2	3.4	1.2	0	6.9	1.2	0	3.1	1.2	1	30.4	5.5	0	30.7	5.3	0
		Thin Film	2/2	2/2	4.2	0.9	0	7.5	0.8	0	4.4	0.8	0	32.1	4.2	0	32.1	5.0	0
Substrate Repackaged (Test No. 231, Group C)	Epoxy	Thick Film	1/1	1/1	3.4	1.2	0	7.7	1.1	0	2.8	0.9	0	31.8	4.8	0	26.1	6.3	0
		Thin Film	2/2	2/2	3.8	1.0	0	7.3	1.4	0	4.4	1.1	3	30.1	7.8	0	28.7	5.0	0

(1) Number of packages passed leak test/total number of packages

(2) Number of packages passed PIN test/total number of packages

(3) $\bar{X}$ = Average pull strength in grams

S = Standard deviation in grams

R = Number of wire loop(s) showing bond electrical resistance increase greater than 0.1 ohm per two bonds experimentally evaluated in this program, regardless of substrate type or package type.

- The reliability of the 2 mil diameter gold wire bonds, to either gold or silver-palladium metallization, was not affected by the replacement of packages in which the substrates were eutectically attached.

- Based on the electrical test results, the reliability of hybrid interconnections involving bimetallic wire bond interfaces is slightly affected by package replacement using eutectically attached substrates. In the non-reworked control group, 11 percent of the wire bonds exhibited a significant increase (by a factor of two in bond electrical resistance), whereas in the reworked group, 24 percent of the wire bonds showed a significant increase in bond electrical resistance.

11.0 THE IMPACT OF REWORK ON HYBRID RELIABILITY

The repair and rework of hybrids has been found by Hughes to be an economical and reliable procedure, and has been practiced for the past ten years. This procedure, if not properly controlled, can significantly degrade product reliability; it was not undertaken without serious evaluation of its impact. Process controls have been continuously applied in hybrid manufacturing in addition to the product tests. Without these controls, rework procedures can result in various types of damage to the hybrid, including:

(1) Mechanical damage to packages, substrates, chips, passive devices, interconnections, and wires;

(2) Thermal degradation of active or passive devices, resistor networks, etc.;

(3) Contamination due to handling, flux residues, improper cleaning, epoxy residues;

(4) Electrical performance changes such as drift, leakage, thermal runaway, frequency response limitations, etc.

All of the above types of damage to the hybrid can result in immediate rejection at the next inspectionpoint or test, or, worse yet, can induce latent failures, that diminish the reliability of the product.

In its most recent effort to fully evaluate the consequences of hybrid repair, Hughes has investigated in great detail the performance and yields of approximately 47,000 high reliability hybrids produced for a major military program in the years 1976 and 1977.[22] Among other objectives, this investigation sought to determine:

(1) The failure modes which cause rework to be performed;

(2) The number of rework cycles to which hybrids are subjected;

(3) The performance of hybrids both during manufacture and in the field;

(4) The handling history and design features of hybrids which exhibit high and low field failure rates.

This study was undertaken to gain understanding of the impact of chip visual inspection and electrical device testing on hybrid assembly and rework. In 1976, a total of 46,811 hybrids of 78 different designs were built for this program. The average hybrid included the following semiconductors:

Diodes	5.2
Transistors	7.0
ICs	2.1
Total	14.3 Semiconductor chips per hybrid

This high reliability line incorporated some unique features which made it effective in the way active devices were handled. These are: 1) devices were procured to stringent procurement specifications imposed on the vendor, 2) a large percentage of active chips were mounted on moly tabs, 3) many critical devices were mounted on TO-5 headers and tested completely prior to installation in the hybrid, and 4) detailed documentation was kept on "travelers" accompanying hybrids. These show all failures, repairs, and rework at every step in the manufacturing cycle. The travelers were reviewed periodically to determine the weak areas of production, and the appropriate corrective action was taken.

The results of these innovations were a very low active device loss, a low rework total, and a low field failure count.

To obtain an accurate picture of device fallout, 5201 assembly "travelers" were reviewed. This represents approximately 11 percent of the total hybrids produced. These assembly travelers included 739 travelers for scrapped hybrids, representing over 40 percent of the total scrapped hybrids. The data were normalized to reflect the actual number of hybrids produced. The percentages of travelers examined varied from 5 to 50 percent of the total production for the individual hybrid types.

Rework of hybrids during assembly. The effectiveness of chip visual examination and electrical testing of chips prior to assembly can also be judged by the amount and type of rework performed on hybrids. The number of rework cycles performed on hybrids is shown in Figure 15. For the hybrid of average complexity of 14.3 semiconductor devices, a record of 68.0 percent initial yield (no-rework) is a remarkable achievement. The

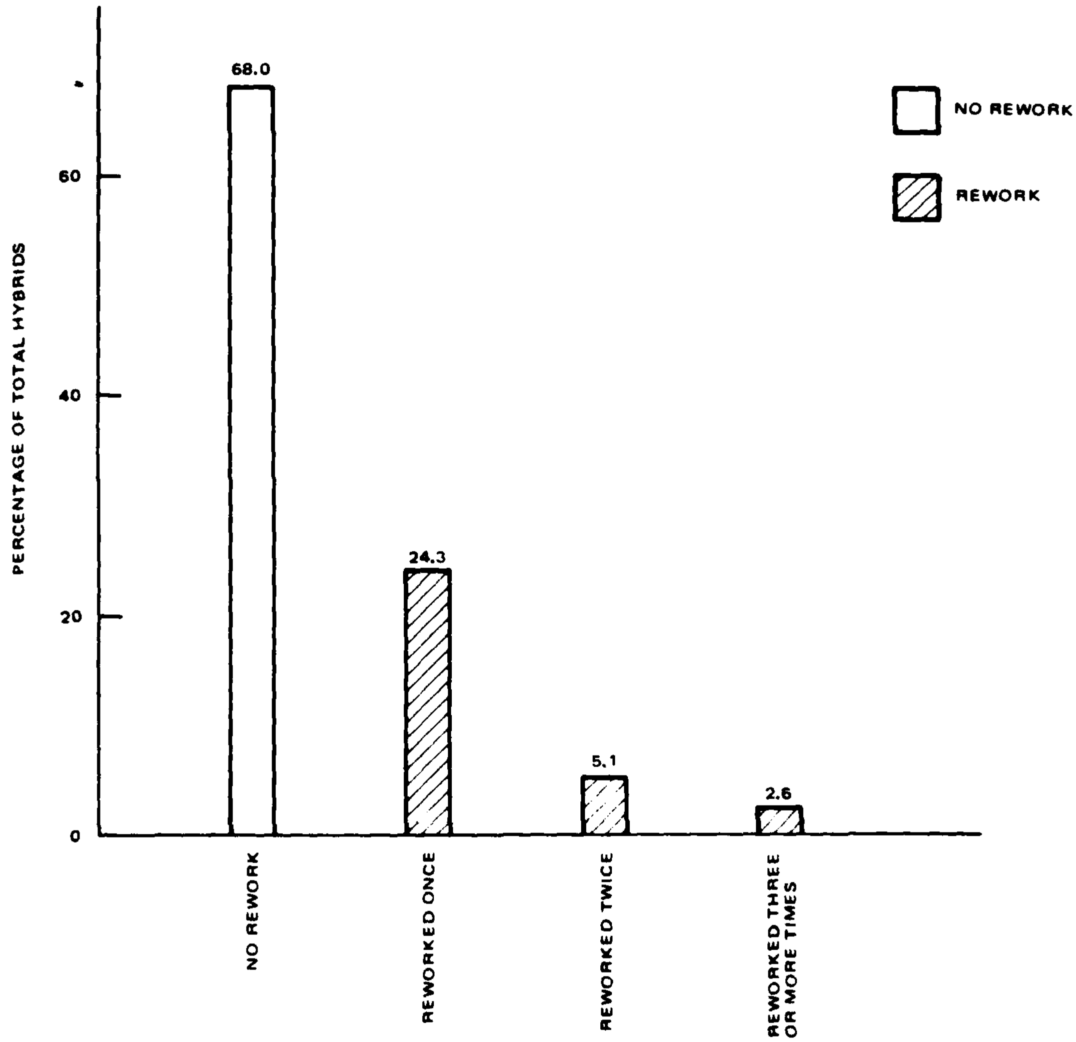

Figure 15. Number of rework operations in assembly of hybrid microcircuits (includes pre and post seal rework).

point of origin of rework, on the production line, is shown in Figure 16. Of the total rework performed, 69.4 percent (22.2 percent out of a total of 32 percent reworked hybrids) was performed prior to package sealing; only 6.3 percent (2 percent of 32 percent) of the rework was due to failing final electrical tests. Since the Pre-Seal Electrical Test was performed prior to any QA examination, the majority of problems were discovered and corrected as soon as the hybrid was made electrically functional.

Figure 17 shows the classification of rework by failure category. The chip electrical failures were 23.9 percent, wire bond-related rework was 23.1 percent, and chip assembly problems were 5.5 percent. The reason

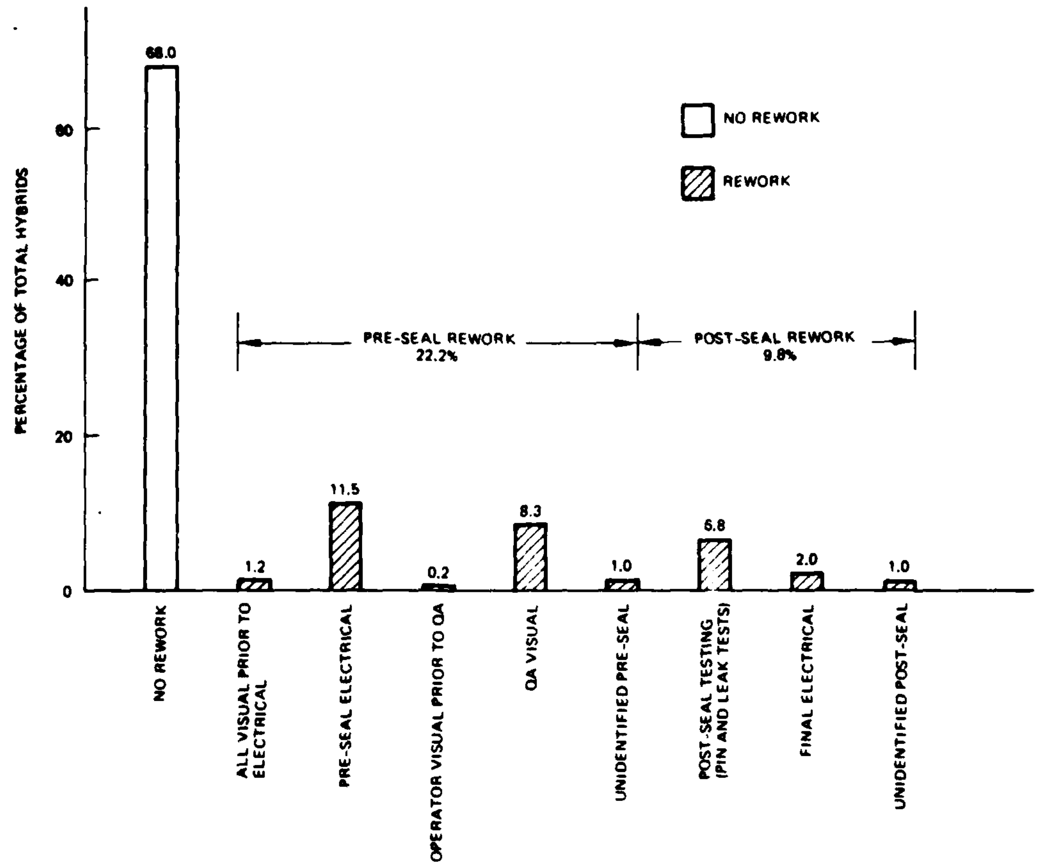

Figure 16. Origin of rework in assembly of hybrid microcircuits.

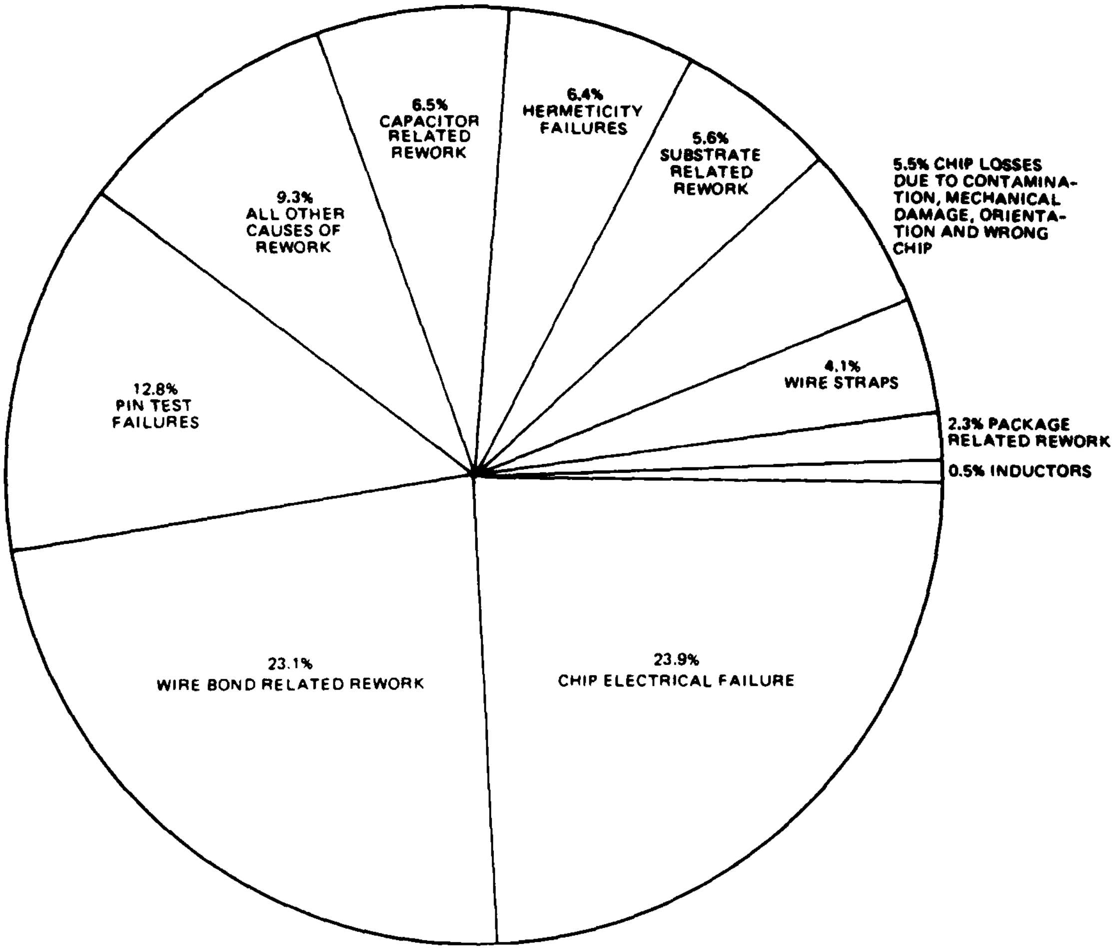

Figure 17. **Classification of rework of hybrids.**

for high wire-bond rework was due to the use of an average of 2.7 prewired transistors per hybrid (PNP and N-channel FET transistors). These transistors required wire dressing. The second major category of wire bond rework was transistors with small bonding pads (3 mil or smaller).

Chip-related rework (including wire bonds) represented over half of the total rework. There was a high amount of rework due to Particle Impact Noise (PIN) test failures.

The total chip related rework was 29.4 percent (23.9 + 5.5). The above data clearly indicate that visual and electrical chip screening results in lower rework and lower active device replacements.

The data from the production line were analyzed to correlate the history of scrapped hybrids with rework. It was found that the average scrapped hybrid had not been subjected to any more repairs or rework than the average accepted hybrid, indicating that excessive rework was not the cause for most scrapped hybrids.

Table 27 shows the data correlating the field performance of hybrids and their previous production rework history. This can be seen by comparing the last column (of field failures per million hours of operation) with the third column from the end which shows the number of reworks per hybrid. Indeed there appeared to be a higher failure rate (8.3 failures per 10^6 hours) for hybrids with high rework ratio (1.33) as compared with the overall average failure rate of 2.3 for the total production average hybrid which was reworked 0.40 times. Yet rework did not appear to be the dominant reason for field failures since parts exhibiting the highest field failure rate (18.2×10^{-6}) had on the average 0.84 reworks/hybrid. The number of reworks per hybrid appears high per unit simply because some hybrids were reworked more than once (includes pre-seal rework).

TABLE 27. SUMMARY OF HYBRID MICROCIRCUIT PRODUCIBILITY AND PERFORMANCE

	Hybrids			Hybrid Complexity (Device Count)									Production and Use Performance			
				Active Chips				Passive Devices								
Hybrid Category	Number of Different Designs	Quantity Produced	% of Total Produced	Diodes	Transistors	ICs	Total	Chip Resistors	Capacitors	Coils	Total	Production Scrap*	No. of Reworks per Hybrid	System Subassembly Returns	Field Failures/ 10^6 hr
High usage hybrids	13	35,995	80.0	5.7	7.3	0.7	13.7	0.1	9.7	0.5	10.3	3.87	0.38	5.9	1.3
High IC die count hybrids	18	3,163	7.0	<0.1	<0.1	18.4	18.4	<0.1	<0.1	0	<0.1	2.69	0.61	8.5	6.6
High assembly rework hybrids	14	1,784	4.0	1.5	5.6	12.3	19.4	0	2.2	0	2.2	6.00	1.33	11.6	8.3
High scrap rate hybrids	31	5,737	12.8	5.4	7.1	4.1	16.6	1.0	13.1	3.2	17.3	8.90	0.81	11.1	4.7
High system subassembly returns hybrids	18	2,547	5.7	4.5	8.4	7.0	19.9	0.4	4.0	0	4.4	4.46	0.67	19.1	6.2
High field failure rate hybrids	18	2,249	5.0	5.7	4.7	9.2	19.6	1.9	1.5	0	3.4	3.60	0.84	9.4	18.2
Total production	78	44,970	N/A	5.2	7.0	2.1	14.3	0.2	8.7	0.4	9.3	3.93	0.40	7.2	2.3

*Data accumulated from 87,380 system operational hours and over 97 million device hours.

NOTE: The predicted failure rate for the above program was 3.0 failures per million operating hours. Calculations were based on the model defined by MIL-HDBK-217B.

12.0 CONCLUSIONS

12.1 Task I - Package sealing rework.

- Resealing of packages, sealed by soft solder and containing polymer attached substrates and devices, does not affect the package leak rate.

- Packages sealed by seam brazing can not be resealed without introducing a high degree of reliability risk associated with the delidding and resealing processes. The probability of a seal failure is very high, resulting in a low resealing yield.

- Rework of seam welded packages is a viable process. Glass bead cracking during the rework process may cause an increase in leak rate. This conclusion should be tempered by the fact that the packages used for this test program have 80 glass-to-metal seals and are quite susceptible to thermal stress cracking of the glass beads. Hughes' experience with other less sensitive seam welded packages has shown that the less sensitive packages can be resealed in excess of five times without failures.

- In resealing packages using soft solder and tinned Kovar bases, a limit of four reseals should be imposed, provided the original nickel film under plating (over Kovar) thickness on the package base sealing surface is at least 200-250 microinches.

- Seam welded packages, with covers removed by milling, may be reliably resealed up to three times. It should be noted, however, that marginal sealing of seam welded packages can result in leak failures during environmental testing. Potential leak sites can be detected by a careful visual examination or by a destructive dye penetrant test.

12.2 Task II - Eutectic device attachment rework.

- Rework of eutectically bonded molytab/chips is limited metallurgically as a consequence of solder oxidation and solder leaching.

- The seal integrity of soft solder sealed packages, containing eutectically attached substrates and devices, can be degraded if the package is thermally stressed during the device rework process. Thermal shock can initiate cracks in the ceramic base of the package.
- During the rework of alloy bonded devices, there is a potential danger of fracturing the glass bead seals of metal packages, the substrate and the base of ceramic packages as a result of thermal shock.
- Damage to other components or devices already on the hybrid substrate is likely due to high rework process temperatures and flux contamination. The materials and circuit elements most susceptible are epoxy adhesives and wire bonds.
- Bonding alloy wetting is more pronounced on thin film gold metallization. The thick film gold surface tends to opnose alloy wetting due to the presence of glass frit and/or copper oxide and surface roughness.
- According to the literature and experimental results from previous studies, the best die-to-substrate metallization bonds are obtained using eutectic alloys (e.g., Au/Si, Au/Sn), whereas the soft solders, such as the Pb-Sn or Pb-Sn-Ag systems, produce unsatisfactory die bonds.[8]
- Higher melting point solder alloys (Sn10) produce the most reliable alloy bonds between metallized chip capacitor terminals and the substrate metallization.
- For alloy attached chip capacitors, the capacitors are less likely to fail electrically or mechanically when bonded to thick film metallization than when bonded to thin film metallization; a high level of electrical/mechanical reliability is achieved using Pd/Ag end terminations.
- Most capacitor chip mechanical failures are caused by a coefficient of thermal expansion incompatibility.

12.3 Task III - Polymer (epoxy) attachment rework.

- An important advantage of epoxy bonding of passive and active devices is that rework is facilitated.
- A major disadvantage of epoxy is that it cannot be used to bond high power active devices, which require a higher thermal conductivity bonding material, such as a hard (or soft) solder.
- A very reliable method of attachment of chip capacitors to substrates is by non-conductive epoxy, using gold wire or gold ribbon interconnects to provide electrical contact. At higher frequencies, the resistance of the gold wire may be significant and have an adverse effect on circuit performance. To eliminate the resistance of the wires and to minimize the incidence of mechanical and electrical failures, the use of higher melting point alloys, such as Sn10, should be considered as the attachment and electrical contact material.
- Experience from the field and results reported in the literature show that epoxies can be used reliably in hybrid microcircuits.
- Epoxy materials must be carefully selected and evaluated to insure reliable performance. The material characteristics considered to be most critical for hybrid applications are: adhesion, electrical stability, metal migration, corrosivity, thermal stability, chemical purity, outgassed molecular species, and effects of outgassed species on device electrical parameters.
- Rework of epoxy attached devices does not influence the reliability of the hybrid. Due to the low process temperatures involved, there is no thermal damage to packages, substrates, devices or interconnections already on the substrate.
- The epoxy bond of replaced devices is as reliable as that of devices not reworked.
- Particle contamination can be minimized through careful workmanship aided by a thorough visual inspection.

- Epoxy contamination on conductors during rework must be avoided. The application of plasma cleaning should be considered as a possible adjunct technique for removing all residual (monolayer) organic films during the rework of wire bonds and devices, after removal of the gross deposits by appropriate (qualified) liquid solvent cleaning procedures.

12.4 <u>Task IV - Interconnection rework.</u>

- The thermosonic gold wire bonding process allows a wider variation in bonding parameters than does thermocompression bonding.

- According to the hybrid manufacturer survey, the most popular method for interconnecting active device chips is the thermosonic process, due to the low processing temperature, tolerance to wide variations in process variables, capability of automation and the retention of gold wire bond strength at elevated temperatures.

- The bond strength of reworked thermocompression gold wire (2 mil diameter) interconnections, both from substrate-to-substrate and from substrate-to-capacitor, were as good as those of the initial bonds. This applies to all substrate types, all device and substrate attachment methods and all package types. The pull strength does not degrade as a result of environmental tests or high temperature storage. Multiple interconnection rework has no affect on the reliability of wire bonds already on the circuit.

- Reworked ultrasonic aluminum interconnections, both from chip-to-substrate and from substrate-to-substrate, on epoxy attached devices or substrates, are as reliable as the non-reworked wires. The pull strength of the reworked or non-reworked bonds is generally better on thin film substrates than thick film substrates. Multiple rework has no effect on the reliability of the wire bonds already on the hybrid circuit. Under severe accelerated test conditions, such as high temperature storage ($150^{\circ}C/1000$ hours), bond electrical resistance may increase, possibly as the result of the formation of gold-aluminum intermetallic compounds and the growth of Kirkendall voids.

12.5 Task V - Package replacement.

- The reliability of the hybrids is not affected by the replacement of packages in which the substrates are attached by epoxy. This applies to all five types of interconnections experimentally evaluated in this program, regardless of substrate type or package type.
- The reliability of the gold wire bonds, to either thick or thin film gold or silver-palladium metallization, is not affected by the replacement of packages in which the substrates are eutectically attached.
- Based on the electrical test results, the reliability of bimetallic wire bonds on eutectically attached substrates is slightly affected by package replacement. Since both the reworked and non-reworked (control) groups exhibit significant increases (by at least a factor of two) in bond electrical resistance, it is possible that premature wire bond failure could result from (a) many repeated high temperature rework cycles, (b) prolonged burn-in at 125°C, or (c) other high temperature/mechanical stresses during environmental testing for acceptance purposes.
- For attachment of substrates to package bases, Sn62 solder and gold/tin eutectic alloy produce a very high reliability bond.
- Thermal expansion differences are not a predominant factor affecting the substrate-to-package bond, although the difference in coefficients of thermal expansion of the attachment materials and the package materials are large.

12.6 General.

- Excessive rework is not the cause of most scrapped hybrids.
- Rework occurs in the hybrid fabrication process when an inspection or test step indicates (a) that a previous process operation has resulted in a condition that is outside the limits of the process or test specification, or (b) a defective part has been used in assembly.

13.0 RECOMMENDATIONS

13.1 Recommended rework processes and controls. To achieve the second program objective, namely, the establishment of rework guidelines that are compatible with state-of-the-art hybrid microcircuits, it is necessary to define in-process controls for use as reliability screening techniques. Ideally, the in-process controls selected should detect failures or expose incipient defects at specific points in the manufacturing process. Rework labor and cost would be minimized considerably if the failures or latent defects were detected prior to package sealing.

Each proposed rework process has therefore been subjected to the following analysis:

(a) Effect of the rework process on hybrid reliability and the degree of risk associated with the rework process.

(b) Determination of rework controls to be imposed in the fabrication and/or test procedures: nature, extent and location of the proposed controls.

(c) Tests required to verify the adequacy and reliability of each proposed rework process.

13.1.1 Package delidding and resealing. Package resealing is considered to be a small but significant source of hybrid failures. In one study conducted by Hughes,[22] 8 percent of the 92 primary field failures of low power hybrids were attributed to package sealing. Of these 8 percent failures, 87.5 percent were caused by solder (shorts from pin-to-pin or from pin-to-substrate conductor) and 12.5 percent were due to cracked glass bead insulators.

The major reliability risks associated with package seal rework, therefore, are:

(a) Electrical shorts due to generation of metal particles during delidding.

(b) Sealing failures due to the use of improper welding/soldering techniques and/or cracked glass beads.

(c) Damage due to chemical corrosion and other thermal or mechanical causes. Flux should not be used inside a hybrid microcircuit package containing mounted active and passive devices. All cleaning processes should be qualified prior to application.

Conductive metal particles and other contaminants are formed during both the lid removal step and to a lesser extent, package resealing. In delidding, the possible effects of the lid removal process on hybrid reliability are given in Table 1 (Section 3). Most loose particles and other contaminants generated during the lid removal process can be removed by cleaning (or immobilized by a conformal coating that permits circuit repair) prior to package resealing. Particles and other contaminants generated during the resealing process, however, are not readily removed by conventional cleaning techniques (or immobilized by a conformal coating).

From the standpoint of the probability of particle generation, the following sealing methods are rated:[1] (a) soft soldering is rated very high, (b) parallel seam soldering, using hard solder ("brazing"), is rated low, (c) parallel seam welding, on the other hand, is rated very low relative to its propensity for metal particle generation.

It should be noted however, that by redesign of the package — lid interface, which requires the use of a special seal joint, it is possible to successfully (manually) soft solder metal packages and significantly reduce the particle generation probability to low.

The proposed rework controls for package delidding and resealing are:

Particle Generation.

It is recommended that PIND testing be utilized on a 100 percent basis for Class B and space grade hybrid microcircuits.

PIND testing may be employed before and after package reseal (and initial seal). A temporary lid may be clamped in place for the preseal PIND test. If particles are detected in the preseal test, they may be removed by various cleaning techniques.[55] Particles detected after package reseal may be removed using the same cleaning techniques, after the lid has been detached. It is not proposed that a nitrogen gas blow be used to dislodge a particle inside the package, since severe damage to interconnect wires may result. Particles not removed by Freon TF should be detached by mechanical means if possible, using such tools as a vacuum probe to lift and hold a loose particle. The utilization of other techniques, such as degaussing, should also be considered. This technique has been recommended to free particles which may be trapped between the pins and the case.

Package seal failure.

Failure of the hermetic seals can be detected by using careful visual inspection of the seal area or the fine and gross leak procedures of MIL-STD-883B, Method 1014.2, test condition A_1 (or A_2 or B) for the fine leak method, followed by test condition C for the fluorocarbon gross leak procedure.

Both the fine and gross leak tests (conditions A_1, A_2, B, C) should be applied after each resealing operation. On parallel seam welded packages, potential leak sites can be detected by a careful visual inspection of the welded seam area. Externally visible seam voids on soft (manually) soldered packages may be eliminated by "touch-up" of the void area, by reflow of the solder, provided the package is baked out prior to solder seal touch up. It is recommended, however, that the lid of the leaking package be removed and replaced by a new lid. If more than one solder reseal is required, it will be necessary for the responsible quality assurance group to determine if the sealing process is still under control. On seam brazed packages, however, elimination of voids by reflow of the solder is not recommended, the package should be delidded, resurfaced and resealed using a solder preform. "Touch-up" of the gold plating on delidded (resurfaced)

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[55] Microcircuit Packaging Free of Loose Metallic Particles, Contract No. F33615-76-C-5273, Fourth Quarterly Report, Report No. P77-404, 1 September 1977, G.T. Malloy, Hughes Aircraft Company, Culver City, California.

braze-sealed metal packages is also not recommended. The package design should be optimized to reduce glass bead failure; the spacing between glass beads should be increased and the distance from the glass bead to the sealing surface should be at least 0.040 inch (0.102 cm).

13.1.2 Eutectic attachment rework. Consideration of the results of the literature survey and the experimental phase of the program yielded a brief listing of in-process controls and screening tests that are applicable to eutectic attachment of active and passing devices. The results of a previous Hughes study[22] showed that active and passive device attachment failures comprised only about 2 percent of the primary field failures analyzed: therefore the effect of this rework process on hybrid reliability in the field is considered to be small.

(a) Thermal cycling (from -65°C to +150°C) followed by mechanical shock (3000 G, Y_1 direction) or constant acceleration was rated as an effective post-sealing screen for detecting bad capacitor chip attachments. Thermal cycling should be applied only after package sealing, however, to prevent moisture or other contamination from damaging the devices and wire bonds inside the package.

(b) Visual examination was of minimal value as an in-process control in detecting marginal capacitor chip attachments.

(c) There is no acceptable pre-seal screen for defective or marginal capacitor chips except constant acceleration or mechanical shock preceded by thermal cycling. Most solder-bonded capacitor electrical failures (about 90 percent) occur after the first mechanical shock (at 3000 G) or the thermal cycling. Literature results indicate that mechanical shock was the environmental test most likely to screen defective chips. Mechanical shock or constant acceleration should be applied after mounting and interconnecting the capacitor chips, as shown in Figure 4 (Section 4.1). Mechanical shock or constant acceleration should be employed as a 100 percent in-process hybrid screen or as a parts and process evaluation test. Thermal cycling (after package sealing) alone is the next best screening test, if mechanical shock is not feasible.

(d) Cleanliness of the substrate and capacitor chips is required for the formation of a good metallurgical bond.

(e) For active devices, a thorough pre-seal visual examination at low magnification (10X - 30X) is considered to be a very effective in-process control for insuring an adequate bond between substrate and device. It is recommended that the area to be inspected be restricted to the fillet around the periphery of the active device chip at the interface (1) between the chip and the metallized substrate bonding pad or (2) between the chip and the metal tab substrate. A uniform, void-free fillet with no particle formation indicates a reliable bond. Visual inspection should be made on a 100 percent basis after die attach.

Soft solder attachment of active device chips is not a recommended process if high tin content alloys are used, such as Sn62. The use of alloys of this type requires the use of flux inside the assembled hybrid. The presence of flux is not acceptable from the standpoint of hybrid reliability after rework.

(f) Constant acceleration testing at 10,000G should be employed only after it has been determined that the test will not destroy the hybrid microcircuit.

(g) Solder voids can often be detected beneath power transistor chips by non-destructive electrical measurements, such as determination of forward-biased second breakdown.[10] This test should be conducted immediately after die attach.

(h) Non-destructive ultrasonic examination of alloy silicon chip-to-substrate bonds has been used to detect interface voids.[20, 21] The ultrasonic test method should be applied after die attach.

(i) In-process control of the die attachment variables can be critical. Collet temperature and substrate temperature are the most important parameters. Optimized die bonder schedules must be established on representative sample chips and substrates as a prerequisite of the bonding of actual production parts. The use of the aforementioned constant acceleration and non-destructive test methods (ultrasonic, forward-biased second breakdown) should also be utilized on a sample basis to optimize the die bonder schedule.

(j) Clean active devices and substrates must be used to insure reliable die-to-substrate bonds. The application of plasma cleaning of substrates, preferably under mild oxidizing conditions, should be considered.

(k) Use of the proper material combinations is also an essential in-process control. The choice of interface alloy is more critical than either the chip backing metallization or the substrate metallization. The choice of proper eutectic or soft solder alloy is determined by the chip backing metallization. It is recommended that an alloy preform be used (with "scrubbing") to prevent voids, especially on larger power device chips. A refractory metal tab or soft solder should also be utilized to prevent cracking of the die (especially of the large power device die). The refractory metal tab and soft solder prevent die cracking by affording a measure of stress relief.

The effect of the eutectic device attachment rework process on in-process hybrid failures is quite pronounced, as determined by the experimental portion of this program. There is a potential danger of fracturing (1) the glass bead seals of metal packages, (2) the substrate, and (3) the base of ceramic packages due to thermal shock. Damage to other components or devices already on the substrate is possible due to high rework processing temperatures and flux contamination. The components most susceptible to damage are epoxy adhesives and wire bonds. If flux is used during rework of eutectically attached devices, it must be removed by an approved solvent, known to be compatible with all components of the hybrid microcircuit.

13.1.3 Polymer (epoxy) attachment rework. The following in-process screens should be considered for active and passive devices bonded by epoxy to thick or thin film ceramic substrates:

(a) Thermal cycling followed by mechanical shock or constant acceleration are considered to be effective environmental test procedures for detecting electrical and mechanical failures of epoxy attached chip capacitors.

(b) For active devices attached by epoxy, a thorough visual inspection of the bond fillet area is the most reliable in-process control procedure. The inspection should be conducted at low magnification (10X - 30X) under a stereomicroscope.

(c) The use of the non-destructive acoustic emission technique should be considered as an in-process screen of the integrity of epoxy bonded (and alloy bonded) chip capacitors on hybrid substrates. The test results reported by Harman(28) indicate that incompletely bonded capacitors can be detected using the acoustic emission method. It is proposed that this screen be applied to production hybrids at least on a sample basis.

In addition to these in-process control methods, a careful evaluation of each epoxy lot is the best reliability screening technique. It is recommended that each lot of epoxy material be evaluated in its specific application under accelerated aging conditions, as suggested by Traeger.(35) (See Section 3.4.6.) Lot qualification tests should include the following:

(a) Mass spectrometric analysis of the uncured resin, to detect any significant concentration of ionizable species that might contribute to a contamination-type failure mechanism.

(b) Infrared analysis of the uncured resin.

(c) Thermogravimetric analysis of the cured resin to detect the presence of unexpected volatile species resulting from incorrect resin formulation and/or inadequate cure.

The effect of the epoxy device attachment rework process on hybrid reliability, as determined in the experimental phase of this program, is not significant. Due to the low process temperatures employed, there is no thermally induced damage to the package, substrate, devices or interconnections already on the substrate. The degree of risk involved in epoxy device attachment rework is considered to be very small.

13.1.4 Interconnection rework. Approximately 32 percent of the primary field failures in low and high power hybrids are attributed to wire bond failures, according to the results of a Hughes study.[22] Wire bond failures are therefore considered to be a major cause of field failures and in-process rework.

The following wire bond in-process controls are recommended as guidelines in the production of high reliability hybrid circuit interconnections using conventional face-up chip and wire processes:

(a) Wire bonding schedules are very important in-process controls. For ultrasonic bonding, force and ultrasonic power are the most critical machine parameters, whereas in pulse thermocompression bonding, temperature and force are the most important variables. In the thermosonic process, the important bonding parameters are ball bond force, temperature and ultrasonic power. It should be emphasized that the thermosonic bonding parameters do not require the rigid processing controls that are characteristic of the pulsed thermocompression process.[14][51] The thermosonic process therefore offers greater process flexibility, which is a major advantage in the production of reliable gold wire bonds.

Destructive pull testing of sample bonds must be performed to establish the optimum bond schedules for the joining of the material combinations. The schedules should be rechecked by making and pulling at least five sample bonds on a test substrate at the start of each shift and at 4-hour intervals thereafter. It is suggested that process control charts (mean and deviation) be kept of the sample pull test data.

(b) Nondestructive pull testing is considered to be the most effective in-process control technique for eliminating marginal bonds. For high reliability hybrids, nondestructive pull tests should be applied on a 100 percent basis.

The double bond-type pull tests should be applied at the conclusion of the wire bonding step, according to MIL-STD-883B (condition D). An applied force of 1 gram is recommended for 1 mil (25.4 μm) diameter gold or aluminum wire and a force of 3 grams is recommended for 2 mil (50.8 μm) diameter gold wire.

(c) Cleanliness of the chip and substrate bonding areas is absolutely necessary for the formation of a reliable bond. The presence of inorganic or organic contaminants may degrade the reliability of the bond. All foreign matter should be removed by the appropriate cleaning process. During rework, using epoxy for device reattachment, the presence of epoxy "bleed out" films on substrate conductors can result in marginal wire bonds.

(d) Visual examination is considered to be of marginal value in the detection of bad wire bonds.

Although it is not a true in-process control, the combination of substrate metallization, bonding process and wire composition is very important in the production of reliable gold and aluminum wire bonds. For example, 1 mil diameter ultrasonic aluminum wire bonds on thin film gold and thick film fritless gold metallization produce a very reliable bond, whereas the aluminum wire produces a potentially weaker bond on thick film fritted gold, as measured after high temperature (150°C) exposure.

The experimental results obtained on this program show that reworked aluminum and gold wires are just as reliable as the non-reworked wires. Multiple rework has no effect on the reliability of the wire bonds already on the hybrid microcircuit. The risk associated with the interconnection rework process is therefore rated low.

13.1.5 Package replacement. When a package is damaged beyond repair (such as a cracked glass seal, a lid seal that cannot be reliably reworked, a broken lead or a cracked ceramic base), it is necessary to open the package, remove the substrate and remount the substrate in a new package.

It is proposed that the following in-process controls be considered for package replacement:

(a) A significant reliability problem occurs in the solder bonding of alumina substrates to package bases. The application of the "vacuum collapse" method has been shown to be very effective in essentially eliminating the thin films of air entrapped between soldered alumina plates.[18]

(b) A very effective method of screening for defective epoxy rebonded substrates is to visually inspect for (1) loose substrates or (2) cracking or peeling of the attachment materials. This inspection should be performed immediately after the substrate attachment step. Certain conductive epoxies cannot be used for attachment of substrates because of the solvent content of the epoxy. During the curing cycle, the solvent outgasses, which causes readily visible voids and cracks to form along the substrate-package interface.

The degree of risk associated with package replacement is considered to be low, based on the test results obtained in the experimental phase of this program. Repackaging of eutectically attached substrates (1) had little effect on device-to-substrate epoxy bonds, (2) did not affect the reliability of pulse thermocompression gold wire bonds, but (3) did effect bimetallic (aluminum wire to gold) wire bonds. The reliability of the test specimen hybrids was not affected by the replacement of packages in which the substrates were affixed by epoxy.

Proper selection of materials is the most effective in-process control. The gold/tin eutectic and Sn62 solder are very reliable alloys for bonding a (bottom surface) metallized substrate to a metal or metallized ceramic package base. Nonconductive epoxy, on the other hand, does not form a strong bond to a metal package surface, which has a much smoother finish than does a ceramic base surface.

13.1.6 General.

1. Rework will be permitted only when hybrid parts are procured according to the requirements of MIL-STD-883B, Method 5008 (Test Procedures for Hybrid and Multichip Microcircuits).

2. In an effort to assess the effects of hybrid microcircuit repair on product reliability, a Hughes Aircraft study has established that the number of reworks per hybrid did not appear to correlate with the number of hybrid system subassembly returns or field failures, that is, a high level of field failures or subassembly returns was not associated with a high frequency of rework.

APPENDIX A

INTERPRETATION OF THE RATIO OF THE STANDARD DEVIATION TO THE MEAN OF THE BOND STRENGTH

According to Harman[52], when the ratio of the standard deviation to the mean of the destructive bond pull strength ($S/\overline{X}$) is equal to (or less than) 15 percent, the bonding process is sufficiently under control to produce high reliability hybrid microcircuit interconnections. For an $S/\overline{X}$ ratio of 25 percent or greater, this value indicates that some aspect of the bonding process (operator, machine or substrate metallization variables) is out of control.

Non-destructive bond pull tests should be used very carefully. For low elongation aluminum wire, the maximum safe non-destructive pull force is $0.9\,(\overline{X} - 3S)$, where $0.25\,\overline{X} \geq S > 0.15\overline{X}$, and the NDP force should be $0.9\,(\overline{X} - 4S)$ when $S \leq 0.15\overline{X}$. No NDP tests are recommended for cases where $S > 0.25\overline{X}$ since this indicates an out of control bonding process.

[52] G.G. Harman, 12th Annual Proceedings, IEEE Reliability Physics Symposium, 1974, pp. 205-210.

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